

# Silicon Thin Films for Mobile Energy Electronics

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This thesis is submitted for the degree of Doctor of Philosophy

I, Arman Ahnood, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

# Abstract

Consumer needs for mobile devices include the requirement for longer battery life, so that recharging can be performed less frequently or eliminated completely. To this end a key component of any mobile system is a high power and high energy density battery. An alternative to better batteries is for mobile devices to harvest some of their own energy. Solar energy is an accessible, free and environmentally friendly source of energy, making it ideal for powering mobile devices.

In this work we present a low deposition temperature (150°C), thin-film solar power harvesting system. Low deposition temperature of thin film silicon and associated alloys allows for fabrication on plastic in order to realize lightweight and robust integrated systems. The system consists of a thin film transistor (TFT) circuit and thin film photovoltaic (PV) array. The circuit functions as a simple DC-DC regulator and maximum power point tracking unit (MPPT).

Amorphous silicon (a-Si:H) is used as the primary thin-film material for the fabrication of the devices. One of the challenges when fabricating devices at low temperatures is the high defect density in a-Si:H due to hydrogen clustering. In here the He in addition to the SiH<sub>4</sub> and H<sub>2</sub> is used to minimise hydrogen clustering. Using the optimised films, TFT and PV devices are fabricated, and analysed.

Low deposition temperatures influence TFT properties. Contact resistance and dynamic instability of TFTs are considered. New extraction methods and their effect on device mobility are presented.

A power conditioning TFT circuit is proposed. A model is developed to analyse the circuit's output stability as a function of stressing and light intensity. System efficiency and its dependence on circuit efficiency and solar cell utilisation are discussed.

The PV array and the TFT circuit are fabricated using lithography techniques, with a maximum process temperature of 150°C. The circuit can provide a degree of output power stability over a wide range of light intensities and stressing times, making it suitable for use with SC. In this work peak system efficiency of 18% is achieved. Despite the circuit's low efficiency, it has the advantage of fabrication on plastic substrates and better integrability within mobile devices.



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"You have 2 choices in life: to find a way or to make one"

*Paulo Coelho*

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# 1 Introduction

## 1.1 Motivation

In recent years there has been a growing interest in mobile and portable computing systems, such as wearable computers, personal digital assistants, smart phones, notebooks, field computers and sensor nodes. Despite the growth in use of wireless connectivity and increased mobile computing, typically a mobile device still needs to be periodically charged and therefore has to have access to an electricity supply network. Furthermore, increase in mobile computing power and communication bandwidth has resulted in higher electrical energy consumption [1], which serves as a limitation to a truly *mobile* system. Today a key component of any mobile system is a high-power and high-energy density battery that can store sufficient energy, be lightweight and compact [1]. It would also need to be safe and environmentally friendly.

An alternative approach to this arrangement is a scheme where the mobile device generates some of its own power thus reducing or eliminating the need for numerous charging cycles. Manual power generation has already been used in some devices. One example of such a device is the XO-1 laptop which is targeted at school children in rural areas, where access to electricity is limited. Below is an extract from an interview given to the BBC news network by one of the XO-1 designers [2]:

*“In areas without access to the grid, various contraptions have been designed to plug directly into the laptop including a solar panel, a hand crank (similar to those used on wind-up radios), a foot pedal and a pull-string recharger, similar to a starter cord on a lawnmower.”*

Some powering schemes, such as manual power generation, would require human intervention. This may not be practical in many applications, where devices are required to operate independently. Solar power is a globally accessible source of energy. It allows mobile devices to operate in remote and inaccessible locations by removing the need for extensive energy delivery infrastructure. Furthermore it is a safe and environmentally friendly source of energy. The solar energy harvesting system captures the solar energy, and uses a circuit to store it in an energy storage unit.

The intensity of the sun light before entering the atmosphere is  $1,300 \text{ W/m}^2$  [3]. After this, depending on the location and atmospheric conditions the sunlight intensity is reduced to values as high as  $1000 \text{ W/m}^2$  [3]. Assuming an average light intensity of  $500 \text{ W/m}^2$ , 5 hours of daylight, a solar cell array area of  $1\text{m}^2$ , and 5% system efficiency, a mobile energy harvesting system can generate and store 125Wh per day. A typical lithium-ion battery cell used in modern laptops has the energy capacity of 60Wh.<sup>1</sup> Therefore, this basic estimate suggests that an energy harvesting system such as this may be capable of producing over twice the amount of the energy stored in a laptop battery in one day. Such a high level of energy, combined with a suitable power management system, has the potential to be a viable energy source for a range of remote devices.

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<sup>1</sup> Dell laptop using a standard lithium-ion battery cell, 4Ah at 15V supply

## 1.2 System Approach

### 1.2.1 Basic requirements

A mobile solar energy harvesting system would require a number of attributes to allow integration with the mobile device it powers. It should be lightweight and durable. A mechanically flexible system would improve the durability and allow better integration. A candidate for such a system is a thin film system fabricated on flexible substrates. Thin film based solar cells can achieve higher power density (power per unit mass) compared with bulk solar cells (such as crystalline silicon). The power density achieved from thin film cells is in the range of 40W/Kg for triple-junction amorphous silicon solar cells on plastic substrate [4].

### 1.2.2 Substrate Selection

Two of the main flexible substrate candidates are plastic and stainless steel. Although stainless steel is compatible with standard deposition temperatures, it would result in a substantially heavier system due to its higher mass density.<sup>2</sup> Plastic substrates are lighter alternatives. The substrate would need to be solvent resistant, so that an optical photolithography process could be used.<sup>3</sup> Additional substrate requirements include low cost (allowing large area mass production), and moisture resistance. Table 1-1 compares properties of some of the plastic films.

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<sup>2</sup> For comparison the density of low grade steel is around 8000 kg/m<sup>3</sup> and 1300kg/ m<sup>3</sup> for a typical plastic substrate, Polyethylene Naphthalate (PEN). Therefore a 0.5mm thick substrate with area of 1m<sup>2</sup> made from PEN would be 0.65Kg compared to 4Kg when steel is used.

<sup>3</sup> Laser scribing is routinely used for solar cell array patterning. However, due to the low melting point of plastic substrates this method is replaced with standard lithography patterning.

<i>Max Deposition Temp. °C</i>	<i>Material</i>	<i>Properties</i>
250	<i>Polyimide (Kapton)</i>	Orange; high thermal expansion coefficient; good chemical resistance; expensive; high moisture absorption
240	<i>Polyetheretherktone (PEEK)</i>	Amber; good chemical resistance; expensive; low moisture absorption
190	<i>Polyethersulphone (PES)</i>	Clear; good dimensional stability; poor solvent resistance; expensive; moderate moisture absorption
180	<i>Polyetherimide (PEI)</i>	Strong; brittle; hazy colour; expensive
160	<i>Polyethylene Naphthalate (PEN)</i>	Clear; moderate CTE; good chemical resistance; inexpensive; moderate moisture absorption
120	<i>Polyester (PET)</i>	Clear; moderate CTE; good chemical resistance; inexpensive; moderate moisture absorption

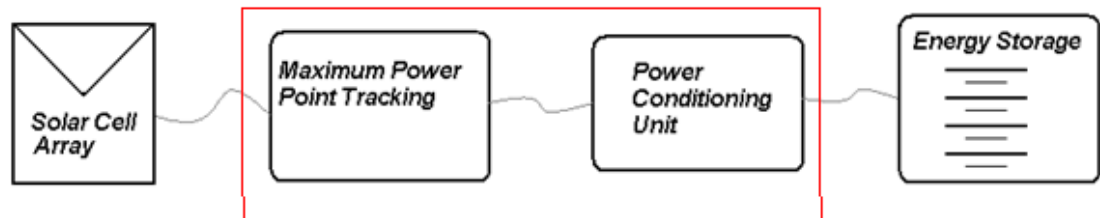
**Table 1-1: Comparison of possible plastic substrates for thin film deposition [5]. In here CTE stands for coefficients of thermal expansion.**

One of the main challenges when using plastic substrates is the substantially reduced process temperature window. The maximum fabrication temperature, shown in Table 1-1, is related to the glass transition temperature above which inelastic deformation takes place and the substrate no longer retains its original dimension. Polyethylene Naphthalate (PEN) satisfies all the requirements and tolerates deposition temperatures as high as 160°C. In this work 150°C is used as the target substrate temperature, to allow for an additional temperature drift of 10°C.

### 1.2.3 Principal Components

Figure 1-1 shows the basic components used in a typical photovoltaic energy system. The solar cell array is an array of interconnected photovoltaic cells, designed to operate close to its optimum operating point, and thus generating maximum power for a given area. A solar cell array operates at a point that depends on its load resistance. However, this operating point is not the point where the array is the most efficient (referred to as the maximum power point).

The maximum power point changes with light intensity. Load resistance can be adjusted so that the cell operates at its maximum power point. The role of the maximum power point tracking (MPPT) is to adjust the load resistance of the PV array such that the array operates at its maximum efficiency. In commercial solar cell modules use of MPPT would result in an increase of efficiency by more than 20% [6]. A number of strategies have been developed for MPPT [7]. MPPT used in this work should be low power, low complexity [8], and be implemented using thin film technology.



**Figure 1-1 Block diagram of a solar energy harvesting system**

A power conditioning unit (PCU) converts the generated electricity to meet the energy storage unit's charging requirements. Therefore the energy storage charging method sets the design requirement for the PCU. Both the PMMT and PCU should be fabricated using thin film technology.

A number of solid phase thin film batteries have been demonstrated [9][10][11]. A common family of thin film batteries is based on lithium-ion [9], especially the ones with polymer electrolytes or lithium-ion phosphate cathodes which have shown good stability [8]. These types of batteries have a high energy density, are environmentally friendly, and require low maintenance. A constant voltage source can be used for charging lithium-ion batteries. However, the life cycle of the batteries is significantly reduced if the charging voltage is not controlled within a narrow range (typically 0.1V for a 4~5V cell) [12]. Therefore using a thin film battery would require a PCU capable

of converting a range of solar cell array output voltages to a constant value. Although this has been implemented using crystalline silicon field effect transistor technologies, its implementation using thin film transistors (TFTs) may be impractical. This is partly due to the large variation in the TFT characteristics and the significant shifts in the threshold voltage during the operation of the TFT.

Thin-film supercapacitors are an alternative approach to batteries [13], as an intermediate power storage unit. Such devices typically have lower *energy* density than a thin film battery [14]. They have higher *power* density, longer lifetime, withstand harsher environments and have less restricted charging/discharge requirements [14][8]. Furthermore, supercapacitors are able to deliver the occasional burst of power as required by many of the power management systems [15]. Supercapacitors with energy volume-density of up to  $25\text{E}4 \text{ Wh/m}^3$  have been achieved [16]. Therefore, to fully store the energy estimated in section 1.1 (125Wh per day) in a capacitor with an area of  $1\text{m}^2$  (the solar cell area), a capacitor thickness of 0.5mm is required. Furthermore, assuming an energy mass density of 4000 Wh/Kg [16], storing 250Wh would only weigh 31.3g. This suggests that supercapacitors are a suitable energy storage unit when integrated with large area devices such as solar cell arrays. This report looks at some of the basic components needed to build a power harvesting system, namely TFTs and solar cells.

#### 1.2.4 Material Selection

The following films are required for the fabrication of solar cells and TFTs; all of which should be deposited at temperatures below  $150^\circ\text{C}$ :

- Intrinsic layer for TFTs;
- Dielectric layer for TFTs;

- Doped contact layer for TFTs;
- Intrinsic layer for solar cells;
- N-type layer for solar cells;
- P-type “window” layer for solar cells.

Organic materials are one possible candidate for this work. However, wide area silicon based thin film technology has been widely used in both solar cells and TFTs. Silicon is cheap, non-toxic, stable, well understood, with a mature manufacturing process. This work considers silicon thin films for both solar cells and TFTs. An intrinsic silicon film has a number of different phases with a range of properties. Table 1-2 compares 3 different phases of thin-film silicon (amorphous, polycrystalline, and micro/nano-crystalline) when used as the intrinsic layers in TFTs and solar cells. Microcrystalline and nanocrystalline silicon are grouped together due to their similar properties.

	<i>a-Si:H</i>	<i>Poly-Si</i>	<i>nc/mc-Si</i>
<i>Growth</i>	Simple; mature growth process	Needs crystallisation of a-Si:H film; complex expensive growth	Slow growth; direct deposition
<i>TFT</i>	Low mobility; unstable	Highest mobility; stable	Medium mobility; stable
<i>Solar Cell</i>	Widely used	High efficiency	Has been used
<i>Low Temp.</i>	Issues at T<150	Not possible	Can be done at T<150

**Table 1-2 Silicon based thin film material for the intrinsic layer**

In this work an attempt has been made to use nanocrystalline silicon as the TFT intrinsic layer. This material shows higher mobility, and better threshold voltage



stability under electrical bias [17]. a-Si:H is used as the absorber for the solar cells due to its higher growth rate<sup>4</sup> and higher absorption coefficient when compared to mc/nc-Si.

### 1.3 Thesis Outline

Figure 1-2 shows an overview of the topics covered in this thesis. As highlighted in the diagram, a number of thin films are shared between the TFT and solar cell devices. The arrangement of the thesis is somewhat different to this overview:

A single chapter, chapter 2, covers all the topics related to the thin film deposition, characterisation and analyses for both TFT and solar cell devices. This chapter discusses the material qualification and optimisation for TFT and PV devices. It starts with a brief review of the deposition tools and material characterisation methods. The transport and growth of intrinsic nc-Si:H is reviewed and discussed. Based on this review, a series of nc-Si:H samples are prepared and characterised. A candidate nc-Si:H deposition condition for use as the channel layer in TFT is identified. N-type nc-Si for the contact layer and SiN are deposited and qualified for use in TFTs. The rest of this chapter discusses the material requirements, growth and characterisation of intrinsic a-Si:H for solar cell applications. Finally p-type a-SiC:H is selected and qualified for use in the solar cell device.

Chapter 3 presents the results of the work on the discrete TFT devices. It discusses the general operation of TFTs and highlights two low deposition temperature effects which influence their behaviour: contact resistance and dynamic instabilities. The fabrication process of the TFTs is discussed and their performance investigated.

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<sup>4</sup> The absorber layer used in the solar cells is typically 100s nm. Therefore the growth rate is more critical than the channel layer in TFTs (typically 10s nm thick)

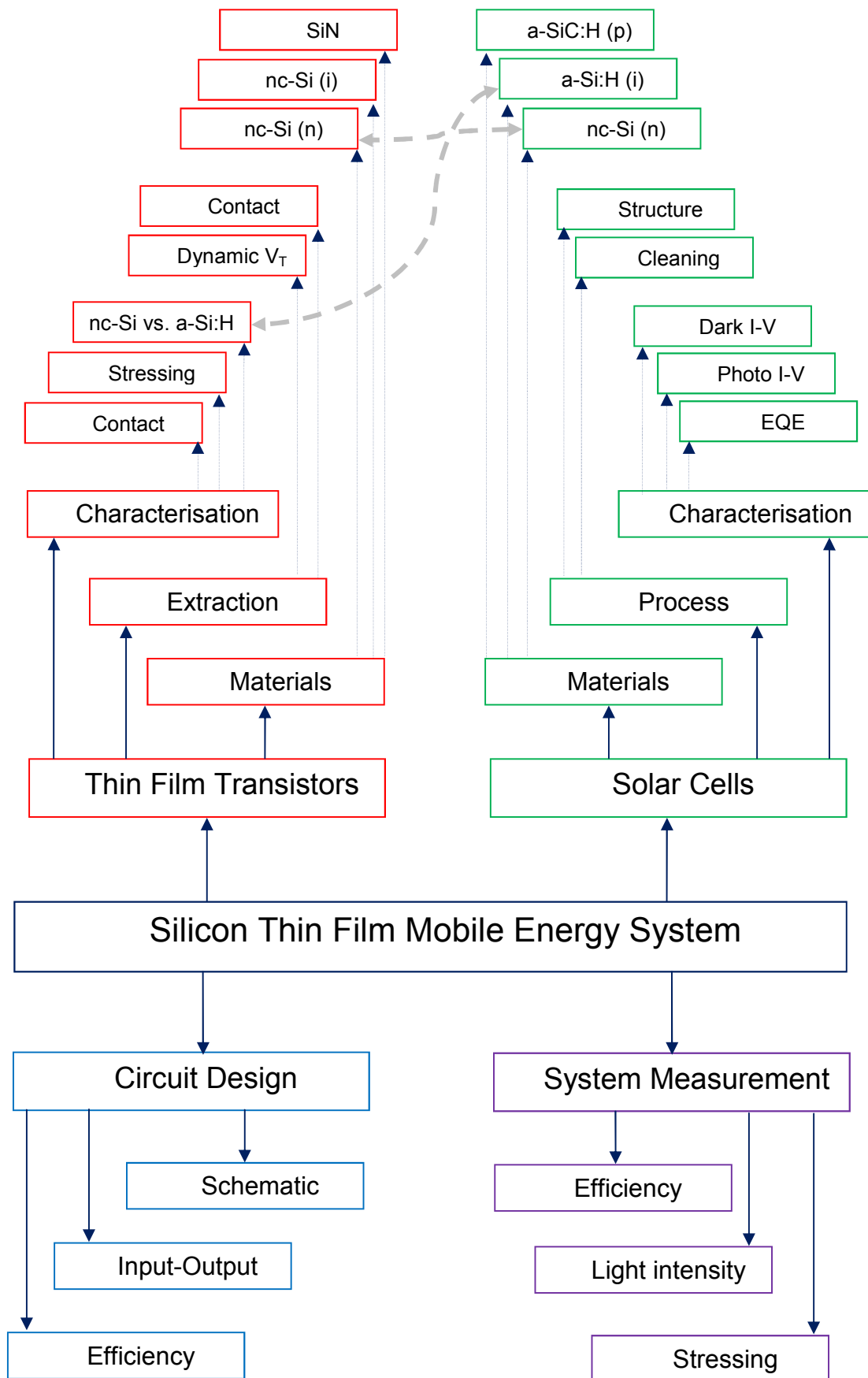


Figure 1-2 Thesis outline

Chapter 4 details the work on the solar cells. It starts by describing the general operation of a p-i-n solar cell. Influences of various parameters on the performance of the device are discussed. Possible device structures are compared and a suitable one selected. The fabrication process, including chamber cleaning to minimise dopant cross-contamination, is optimised. Detailed characteristics of an optimised device is presented and discussed.

Chapter 5 deals with the system design for the mobile energy harvesting system. It describes the circuit adopted for this work. Analysis of the circuit operation and characteristics are presented in this chapter. This chapter also presents the circuit and solar cell array layouts and the fabrication processes for the solar cell array.

Chapter 6 discusses the results of the mobile energy harvesting system. It starts with the characterisation of the solar cell array fabricated using photolithography. The performance of the solar cell array is compared with individual solar cells, fabricated using the standard process described in chapter 5. The solar cell array is then connected to the TFT circuit and a capacitor. The properties of the integrated system are then investigated and examined.

Chapter 7 concludes this thesis. Based on the results of this work, the system suitability for powering various mobile devices is considered. A number of recommendations for further work are made.

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## 2 Materials

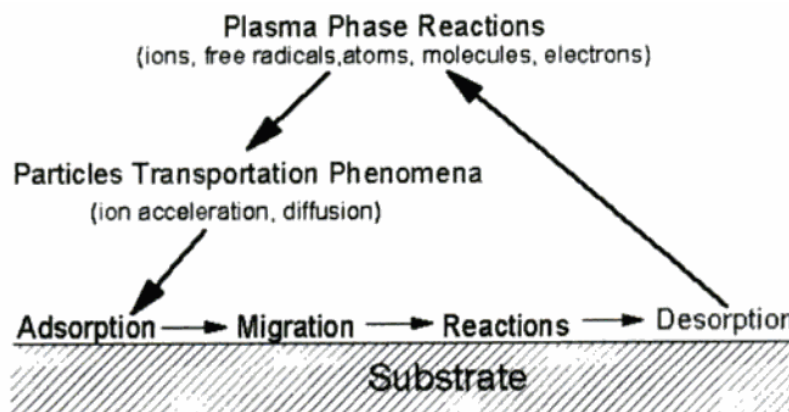
### 2.1 Deposition Tools

#### 2.1.1 Plasma Enhanced Chemical Vapour Deposition

Silicon thin film deposition methods can be grouped in two general categories:

- Physical Vapour Deposition (PVD): atomic species arrive at the substrate and are deposited. By controlling the substrate temperature, some movement and rearrangement of bonds are possible, but no chemical reaction takes place at the substrate. PVD is generally safe as it does not use a gas source, requires ultra-high vacuum, and has a slow growth rate with mono-layer control. This method is not suitable for large area devices due to the difficulty in achieving uniform films.
- Chemical Vapour Deposition (CVD): ionic species chemically react at the surface of the substrate leading to the deposition of thin films. Figure 2-1 simplifies some of the processes which take place in a CVD system. The CVD generally uses hazardous gases as the source material, requires lower vacuum and therefore lower capital costs. CVD is faster at the expense of lower control

over thickness. It is suitable for large area fabrication due to more homogenised species in the chamber.



**Figure 2-1 Simplified CVD deposition processes. Taken from [18]**

Normally the CVD method is used in silicon solar cell and TFT fabrication as it also results in better material properties. There are a wide variety of CVD methods, depending on the method of converting the gas source to ionic species, and delivering the ionic species to the substrate. Two of the most widely used methods are:

- Radio Frequency (RF) Plasma Enhanced Chemical Vapour Deposition (PECVD): plasma is generated by decomposing gas into ionic species, using an ac-bias. This method has widely been used for deposition of thin films used in solar cells and TFTs.
- Hot Wire Chemical Vapour Deposition (HW-CVD): the gas is decomposed into ions thermally using a wire heated to a high temperature. There is an interest in this method from the solar cell community due to its high growth rate and its ability to produce solar cells with low light induced degradation[19][20].

In this work the RF-PECVD deposition system is used. The excitation source is an RF generator with frequency of 13.45MHz. The PECVD system used in this work

consists of two deposition chambers connected to each other through a load lock. One of the chambers is used for the growth of intrinsic silicon based thin films. The second chamber is used for the growth of doped and insulating films. Separating the intrinsic and doped/dielectric chambers eliminates the problem of cross contamination, leading to a higher quality intrinsic film [21]. In the “dirty chamber”, a “dummy run” of a-Si:H is performed (equivalent to 300nm film) to reduce the effect of cross contamination between different types of doped and dielectric films [21]. The substrate can be transferred between the two chambers under vacuum, allowing the deposition of multiple layers of film without exposing their interface to the atmosphere and thus achieving better quality devices and a more controllable process.

Figure 2-2 shows the schematic overview of one of the PECVD chambers used in this work. A turbomolecular pump with backing rotary pump and nitrogen bleeder is used to maintain a chamber base pressure of 1  $\mu$ Torr or less. This is necessary to prevent contaminants from the atmosphere such as oxygen which can act as a dopant in silicon films [22].

A resistive heater inside a stainless steel well is used for substrate heating. This approach is used so that the heater is not in the chamber and therefore it does not act as a contamination source. The heat is transferred from the heater to the stainless steel well, and then by radiative transmission to the substrate. The temperature is measured at the heater well (i.e. outside the chamber) using a thermocouple. The temperature of the thermocouple is calibrated against the temperature of the substrate for the range of interest (50°C to 500°C by the manufacturer and 100°C to 200°C with an error of  $\pm 6^\circ\text{C}$  by me). This calibration is used throughout this work. The effect of additional heating during the deposition is neglected [23].

Gas mass flow controllers have errors of  $\pm 0.1$  sccm for gases with a low flow rate setting (i.e.  $\text{SiH}_4$ ,  $\text{B}_2\text{H}_6$ ,  $\text{PH}_3$ ) and  $\pm 1$  sccm for gases with a high flow rate setting (i.e. He,  $\text{H}_2$ ,  $\text{N}_2$ ,  $\text{NH}_3$ ). Different gases are used in the intrinsic and dirty chambers. The gas is fed into the chamber from the side wall, through a series of valves and mass flow controllers. Using a side wall feed approach at high gas flow rates and low deposition pressures results in a significant pressure drop across the chamber, in the direction of the gas flow. This is a major problem for larger chambers resulting in a nonuniform film growth [24]. A better alternative is a 'shower head' gas feed through one of the electrodes. However in the absence of this, for small chambers, higher pressure can be used to minimise the effect of pressure drop across the chamber and improve the film uniformity [24]. Throughout this work the relation between the pressure and flow rate is considered when choosing deposition conditions.

The substrate is placed on the grounded electrode which is vertically above the RF plate. This is done to reduce the possibility of debris falling on the substrate during the deposition. The RF generator is equipped with an automatic matching circuit to minimise the reflective power. It is also capable of measuring the plasma self-bias voltage. This voltage is an indicator of change in plasma condition during the deposition. Typically a large drift in plasma voltage is an indication of change in plasma uniformity [25], which may indicate a non-uniform film growth.

Regions of stable plasma were investigated by measuring drift in the plasma voltage during the initial 10mins of deposition under a range of RF powers and pressures. The gases used were  $\text{SiH}_4$  (2sccm) and  $\text{H}_2$  (200sccm); a typical gas flow ratio for nanocrystalline silicon (nc-Si:H) [26]. Figure 2-3 and Figure 2-4 show the variation in



the plasma voltage. Points shown with red squares and black outlines indicate failed attempts to ignite the plasma (after 5 attempts).

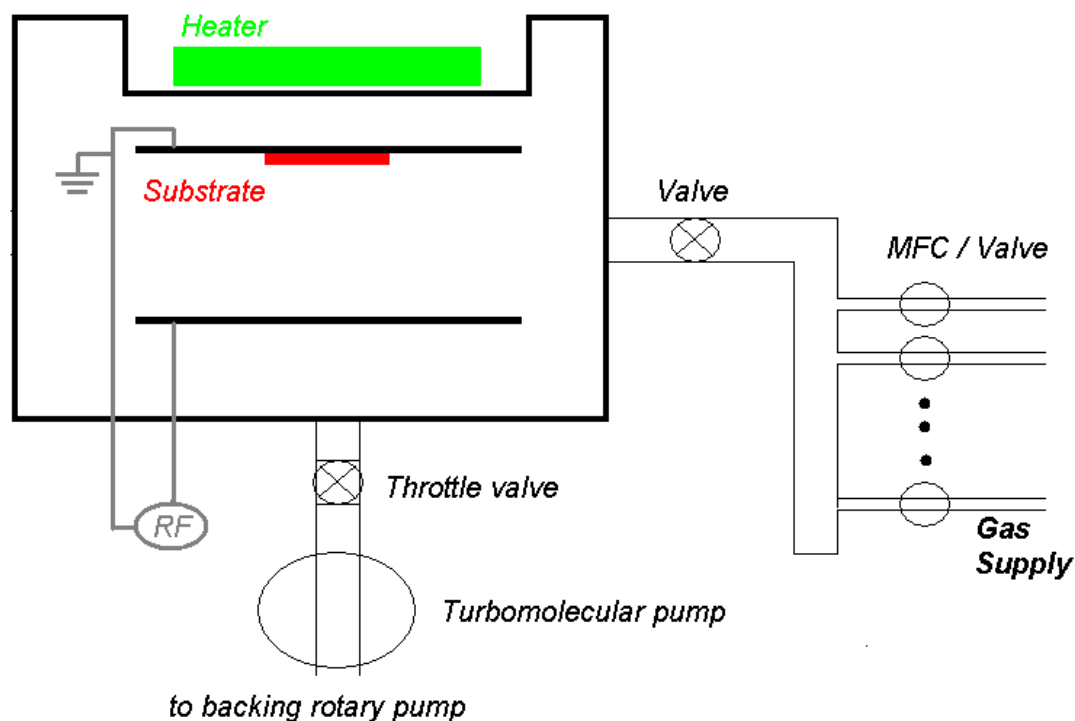


Figure 2-2 Simplified schematic of the one PECVD deposition chamber

Two observations can be made from the graphs. Firstly, plasma voltage drift in PL3 (the “dirty chamber”) is larger than the change in PL2 (intrinsic chamber). The difference may be due to different chamber designs, as PL2 is designed to work at a higher frequency as well as radio frequency. Secondly, the graphs show a larger change in the plasma voltage in higher pressure and higher power operation and this should be avoided. This is only a preliminary consideration and further optimisation is done when individual films are deposited.

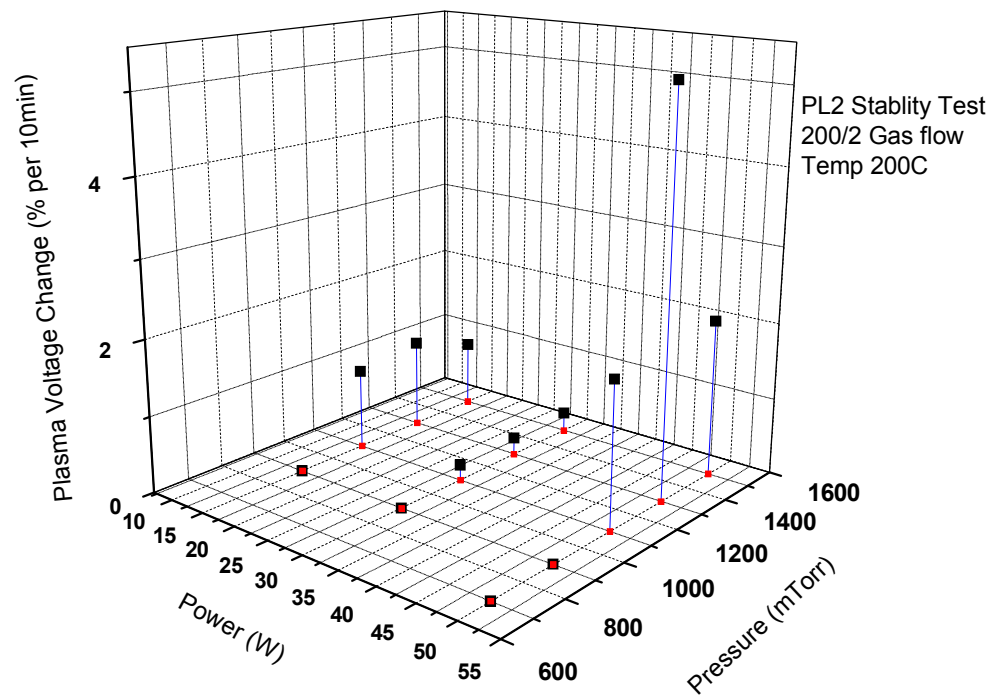


Figure 2-3 Stability of plasma voltage in the intrinsic chamber, PL2

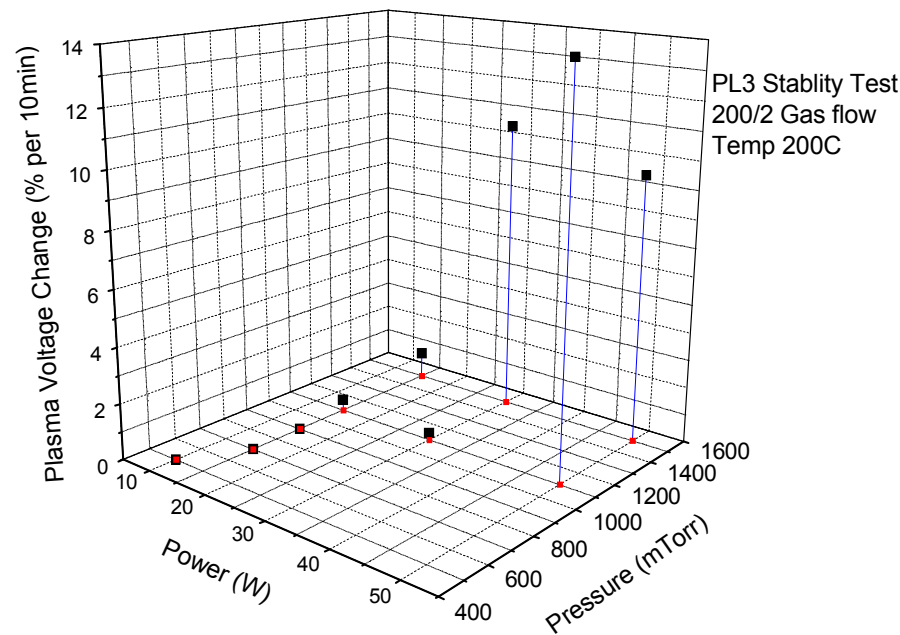
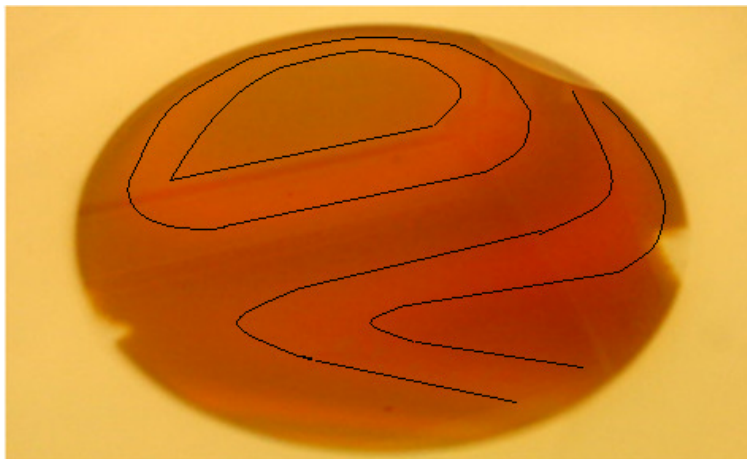


Figure 2-4 Stability of plasma voltage in the contaminated chamber, PL3

A sample with unstable plasma voltage (close to two times variation) is shown in Figure 2-5.



**Figure 2-5 An example of non-centric non-uniformity accompanied with large shift in the plasma voltage. The superimposed contours highlight the colour variation due to thickness non-uniformity.**

### 2.1.2 Evaporators

Two types of evaporators were used for the deposition of metal layers: an electron-beam (e-beam) evaporator and a thermal evaporator. In this work the e-beam evaporator was used for the evaporation of thin (less than 15nm) gold and titanium films. Finely controlled and low evaporation rates could be achieved using the e-beam evaporator. The thermal evaporator was used for the evaporation of aluminium and chromium.

A thickness monitor (based on a quartz crystal resonator) was used to monitor the evaporation rate and the thickness of the films. Typical evaporation rates for gold and aluminium were 0.01 nm/s and 0.1~0.5 nm/s respectively. A shutter was used to stop the evaporation when the desired thickness was reached. A dummy glass substrate was placed next to the sample and the film thickness and sheet resistivity were measured after each deposition step.

Both evaporators were connected to turbomolecular pump. A vacuum level of better than  $1\text{E-}6$  mBar was achieved before performing the evaporations. Both evaporators had rotary substrate holders to minimise any non-uniformity due to the point-source metal. Furthermore due to the large separation between the metal source and the substrate good uniformity was achievable.

## 2.2 Characterisation Methodology

### 2.2.1 Raman Spectroscopy

Raman spectroscopy is a powerful, non-destructive tool which has widely been used in material research. In this method the sample is excited with a laser light, some of the light is absorbed, and the rest is scattered. Most of the scattered light would have the same wavelength as the laser, Rayleigh scattering, but some would interact with phonons, resulting in a small shift of wavelength, corresponding to the vibrational energy state of the material. Depending on whether a phonon is absorbed or emitted, the Raman scattering can be Anti-Stokes or Stokes. The relative intensity of the Stokes and the Anti-Stokes is temperature dependent and as temperature is reduced the Stokes signal becomes stronger. At room temperature the Stokes scattering is stronger and easier to detect.

Raman spectroscopy has been used on silicon thin film to detect material stress, crystal size and crystal volume fraction. The Raman shift of amorphous silicon is a broad Gaussian peak centred at  $480\text{ cm}^{-1}$ , and for crystalline silicon it is a sharp Gaussian peak centred at  $520\text{ cm}^{-1}$  [27]. Raman spectra of nc-Si:H (mixed phase material) would consist of a combination of these two peaks. Grain boundaries may also give rise to an additional peak at close to  $510\text{ cm}^{-1}$  [28]. Although the effective media

theory is often used to calculate the crystal volume fraction, this approach is affected by a number of factors, as outlined below:

- The quantum size effect results in a shift of Raman peaks towards lower wavenumbers for smaller silicon crystal sizes, based on the following relation[29]:

$$\Delta\omega = -A\left(\frac{a}{D}\right)^\gamma \quad (2.1)$$

where  $\Delta\omega$  is the shift in wavenumber,  $a$  is the lattice constant of silicon, 0.357nm,  $A=47.41\text{cm}^{-1}$  and  $\gamma = 1.44$ . It should be noted this relation is based on the assumption that the crystals are spherical, which may not be true for nc-Si:H, as there is a large amount of evidence for columnar PECVD growth[30].

- The peaks are shifted towards lower wavenumbers if the material is under tensile stress [31].
- There is evidence for a distribution of crystalline grain sizes, as opposed to single grain size, leading to an asymmetric Gaussian peak extended into lower wavelengths.

Given that Raman spectroscopy combines all the information together, it makes precise parameter extraction difficult. In this work, the precise nature of nc-Si:H is not investigated. Raman spectroscopy is used as a semi-quantitative measurement tool [31], to investigate the crystal volume fraction and obtain qualitative information about the crystal size in the sample. The following equation is used to extract the crystal volume fraction [27]:

$$X_C = \frac{I_C + I_{GB}}{I_C + I_{GB} + \alpha I_A} \quad (2.2)$$

In the equation above  $I_A$  is the amorphous part of the signal, defined as the area under the  $480\text{cm}^{-1}$  peak.  $I_C$  is the crystalline component, defined as the area under the sharp peak at  $520\text{cm}^{-1}$  or close to it.  $I_{GB}$  is the grain boundary signal and is attributed to the peak at  $510\text{cm}^{-1}$ .  $\alpha$  is the ratio of phonon scattering cross sections of crystalline silicon to amorphous silicon. A value of 0.8 is adopted as used in [27]. A green laser is used here because its penetration depth is comparable to the sample thickness. As this work focuses on low process temperature samples, minimal laser power is used for the excitation to avoid oxidation, and crystallisation due to localised heating of the sample. A number of measurements are taken and averaged to improve the signal-to-noise ratio.

### 2.2.2 Room Temperature Conductivity Measurement

Conductivity measurement is a simple non-destructive measurement which can be performed in dark or light (typically  $100\text{mW/cm}^2$  light source) conditions. Although it is difficult to directly extract the material properties of a sample from this measurement, it can be used to compare samples and judge their suitability for use in the devices.

Despite its simplicity, this measurement can be significantly affected by error. The state of the film surface results in band bending near the surface of the film. Unless the film is sufficiently thick, the band bending would extend into a large portion of the film and the measurement would be a function of the film's surface and not the bulk of the film itself. This can lead to orders of magnitude error for films below  $100\text{nm}$  [32] for intrinsic a-Si:H.

a-Si:H film thickness of 300nm has been widely used as a compromise between surface state error and the need for uniform illumination in photoconductivity measurements [21]. However, it is well known that, unlike a-Si:H, the structure of nc-Si:H film changes with thickness. Also, nc-Si:H films used in some devices (such as the thin p-layer in solar cell or i-layer in the TFT) are very thin.

This leads to a predicament: on one hand, measurement of thin films results in a surface effect error, and on the other hand the thicker films would have different structural (and hence conductivity) properties from the film used in the devices. There is no *correct* approach to this problem. A survey of the recent work on nc-Si:H conductivity [33] suggests that the surface effect error is neglected. For consistency and comparability of the results this approach is used in this work. However, a systematic attempt is made to minimise the surface state effect. Samples are exposed to air at low temperatures ( $<30^{\circ}\text{C}$ ) after deposition, to minimise surface oxidation, and measurement is done on fresh samples (less than a day old). Dark conductivity is performed before photo conductivity to avoid trapping photocarriers in the surface oxide.

Gap cell structures with a length of 10mm and width of 1 or 2 mm are used for contacts. Contacts are 50nm thick thermally evaporated chromium films. The measurement is performed using a Keithley 4200-SCS semiconductor parameter analyser with a voltage range of -50V to +50 V. A dual sweep is performed to look for any possible hysteresis related errors (e.g. RC time constants). If needed, the measurement time setting is increased to minimise hysteresis.

### 2.2.3 Transmission-Reflection Measurement

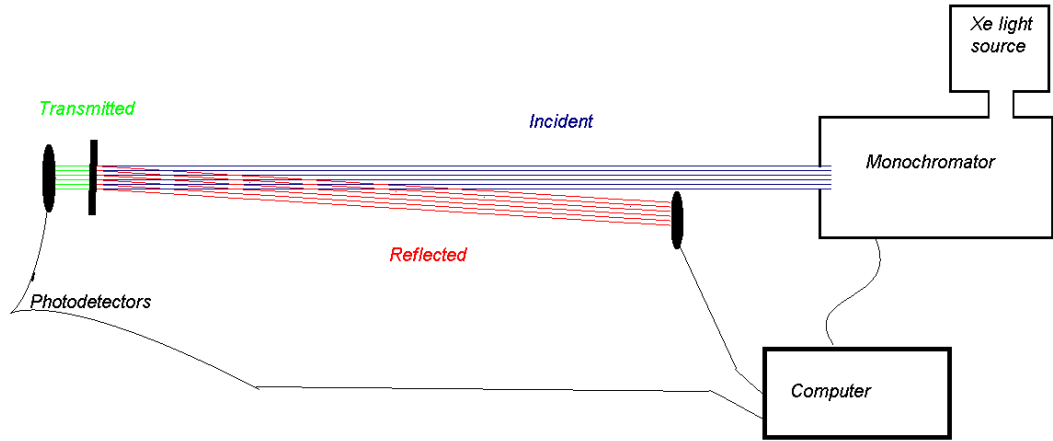
Optical bandgap is an important film parameter for material characterisation. Silicon thin films can have a range of optical gaps from 1.1eV for large grain microcrystalline

silicon to 2.0eV for small grain nc-Si:H. Furthermore, silicon can be alloyed with other materials such as germanium or carbon to extend its bandgap range even further. The optical gap is also an important design parameter for the window layer and absorber layer of the solar cells.

The absorption spectrum of the film is used to extract the optical bandgap. There are two optical approaches for calculating the absorption spectrum. One approach is to measure the transmission and the incident light intensity and assume the difference is due to absorption. This approach is justified when measuring thick films where the absorption is more significant than the reflection. However, in this work films as thin as 20nm are investigated. Therefore, for better accuracy in the absorption spectrum extraction, reflection is measured as well. Figure 2-6 shows the transmission-reflection measurement set-up used to measure the absorption spectrum. The light source is a broadband white light source (Newport 75W Xenon lamp). The monochromator is fitted with gratings in the ultraviolet-visible (180-650nm) and visible-infrared (450nm-1400nm) range and is calibrated using a laser.

The transmission detector is a silicon “pyrodetector” (photodiode) optimised and calibrated for use in the ultraviolet-visible-IR (190nm-1100nm) range. A standard silicon photodiode is used for the reflection measurement due to its small footprint. The monochromator is controlled using a computer, which facilitates the automatic sweep of wavelengths. The output of the pyrodetector and photodiode is recorded by the computer for each wavelength. During the measurement a red filter (600nm) is used to remove the monochromator’s second harmonics when the measurement is performed at wavelengths longer than 600nm. The red filter and additional lenses are used to focus the light but are omitted from Figure 2-6.





**Figure 2-6 Transmission-reflection measurement set-up**

Using this set-up, the transmission-reflection measurement requires 5 sets of measurements: transmission through the substrate ( $T_{\text{substrate}}$ ); reflection from the substrate ( $R_{\text{substrate}}$ ); transmission through the sample and substrate ( $T_{\text{sample}}$ ); and reflection from the sample and substrate ( $R_{\text{sample}}$ ). The sample is replaced with a wideband mirror ( $R > 90\%$  for 250nm to 600nm) for measurement of incident light ( $I_{\text{incident}}$ ). The reflection and transmissions are calculated using the equations 2.3 and 2.4 respectively.

$$R = \frac{R_{\text{sample}}}{I_{\text{incident}}} \quad (2.3)$$

$$T = \frac{T_{\text{sample}}}{T_{\text{substrate}}} \quad (2.4)$$

From this information the absorption can be calculated using the equation (2.5).

$$\alpha \approx -\frac{1}{d} \ln \left[ \frac{T}{1-R} \right] \quad (2.5)$$

Where  $d$  is the sample thickness in cm. The Tauc equation, shown below, and the Tauc plot relate the absorption spectrum to the optical bandgap [34].

$$\hbar\omega\alpha = A(\hbar\omega - E_T)^2 \quad (2.6)$$

$\alpha$  is the absorption as a function of photon energy,  $\hbar\omega$ , and  $E_T$  is the bandgap.  $A$  is a constant. Using the Tauc equation for calculating bandgap is liable to interpretation error as it is only a limited case approximation for two parabolic band edges [34]. An alternative method of defining the optical properties is by measuring the  $E_{04}$  wavelength, which is defined as the wavelength where the absorption is  $10^4 \text{ cm}^{-1}$ . The latter method is less susceptible to interpretation error, although it is affected by film thickness measurement error. In this work both of the parameters are measured for comparison with other works, as they are both used in literature [35].

#### 2.2.4 Constant photocurrent Measurement

Figure 2-7 shows the three different regions of the full absorption spectrum of a semiconductor. Strong absorption takes place in region A, where photon energies are larger than the bandgap. The absorption in this region can be measured using the reflection-transmission measurement described earlier. In region B absorption is due to the band-tail states and drops exponentially with reduction in the photon energy. For a low defect amorphous silicon film, region B is generally observed in the 1 to  $3000 \text{ cm}^{-1}$  range [34][36]. The exponential slope in this range can be described by the equation

below where  $E_u$  is the Urbach energy [34]. Urbach energy is an important material parameter and indicates the transition from the band-tail to the mid-gap states.

$$n\mu\tau = \frac{I_{photo}W}{eVl} \cdot \frac{1}{F(1 - R_f)(1 - \exp(-\alpha \cdot t))} \quad (2.7)$$

In region C absorption is due to the mid-gap states, with lower values of absorption indicative of a lower density of mid-gap states [37]. The free carrier absorption effect is neglected for intrinsic a-Si:H due to the low density of free carriers.

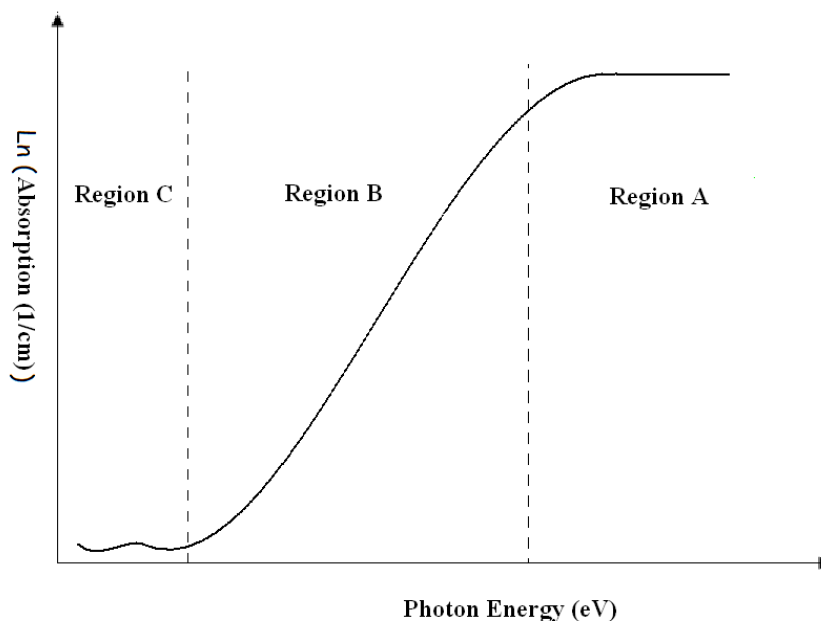
The transmission-reflection method may be used to measure the absorption in region A. Due to weak absorption in regions B and C alternative measurement methods are employed. Four common methods are the photothermal deflection spectroscopy (PDS), the photoacoustic spectroscopy (PAS), the constant photocurrent measurement (CPM) and the dual beam constant photocurrent measurement (DB-CPM). PDS is based on the detection of thermal energy by the sample when exposed to sub-bandgap light. This makes this method suitable for thicker films [38]. In addition to this, impurity related photo absorption by the electronics grade Corning glass leads to errors in the PDS measurements [39][40].

Typically in PDS experiments thermal energy variation is detected by immersing the sample in a suitable liquid (e.g.  $CCl_4$  [41]) and measuring its change of refractive index using a probe light beam and position sensitive detector. PAS also uses thermal energy measurement to detect photo absorption in the sub-bandgap states. However unlike PDS, PAS uses acoustic waves, generated by the change of pressure in the ambient gas, to detect thermal energy [42]. This is achieved by pulsing the pump light beam to heat the film, thus creating acoustic waves in an ambient gas. As with the PDS, PAS relies

on the detection of thermal energy, making it unsuitable for thin films and glass substrates. Furthermore it has been suggested that PAS is less sensitive than CPM by a factor of 100 [43].

An alternative to the detection of absorption using thermal energy is the photocurrent measurement. However variation in the photocurrent measurement does not directly correlate with the variation in absorption coefficient. This is because carrier lifetime ( $\tau$ ) does not remain constant at different photocurrents, due to the  $\tau$  dependence on the quasi-Fermi level position. A solution to this problem is to maintain the same photocurrent, by adjusting the light intensity across the measurement spectrum. This approach is used for both CPM and DB-CPM.

CPM is only sensitive to the photo absorptions which leads to carrier transition into extended states and excludes the transitions which lead to localised states. In DB-CPM in addition to a pulsed monochromatic probe light, the sample is subjected to a pump light bias. This allows the formation of quasi Fermi levels above the deep defects levels leading to a more accurate picture of the deep defect states [44]. Despite its limitations CPM is commonly used to characterise sub-bandgap absorption and this method is used in this work.



**Figure 2-7 Absorption spectrum of semiconductor films**

Figure 2-8 shows the constant photocurrent measurement set-up used in this work. A voltage source is used to provide 10V~20V across an evaporated chromium gap cell with a separation of 1 or 2mm. A chopper is used to modulate the monochromatic light and a digital lock-in amplifier, in current-sense mode (i.e. with an internal resistor), is used to detect the modulated photocurrent. The frequency of the chopper is set at 13 Hz, to avoid any interference from the power line harmonic and allow for the slow states to respond.

The photocurrent is maintained at a constant level for all wavelengths by adjusting the intensity of the light using a neutral density filter wheel. This attenuated light's intensity is measured using a beam splitter and a silicon photodetector. Using this method the intensity of the attenuated light as a function of wavelength is measured in all three regimes, from 2eV to 1.4eV or lower. Absorption is inversely proportional to the intensity of light required to maintain a constant photocurrent. Region A is used to

calculate the proportionality constant using the CPM and transmission-reflection measurement data.

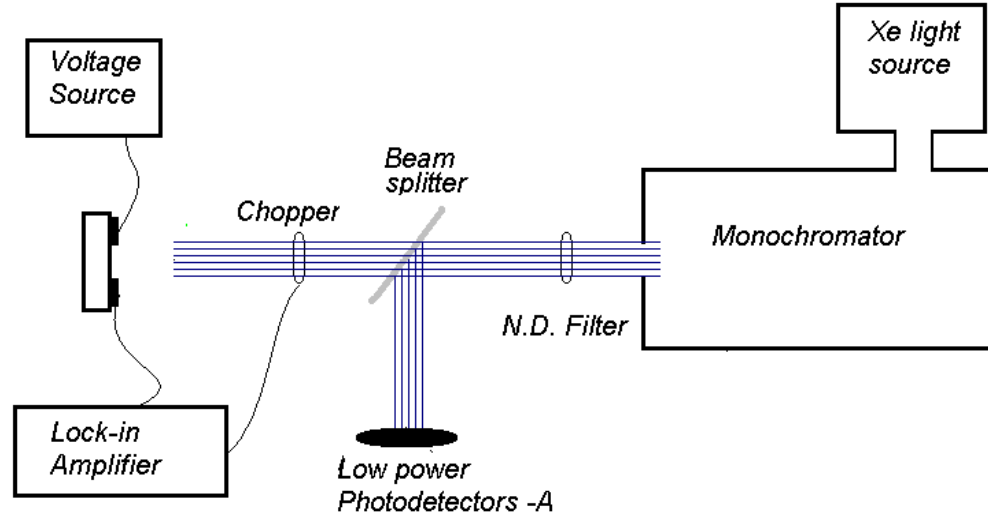


Figure 2-8 Constant photocurrent measurement set-up

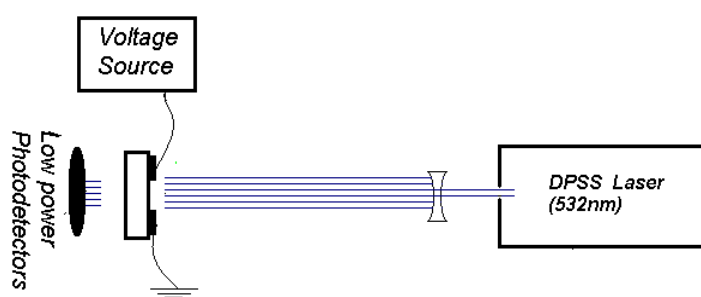
### 2.2.5 Steady State Photoconductivity

The probability of collecting the generated photocarriers is influenced by the mobility of the carriers,  $\mu$ , and their lifetime,  $\tau$ . The mobility-lifetime product,  $\mu\tau$ , is an important thin film property, especially for solar cells. This value can be measured using primary steady state photoconductivity measurements. In this method, the photon flux absorbed by the film and the corresponding photoconductivity is measured. These values are used to calculate the mobility-lifetime product using the equation below [36]:

$$n\mu\tau = \frac{I_{photo}W}{eVl} \cdot \frac{1}{F(1 - R_f)(1 - \exp(-\alpha \cdot t))} \quad (2.8)$$

$n$  is the quantum efficiency for carrier generation, commonly assumed to be 1;  $F$  is the intensity of incident light;  $R_f$  the reflection;  $\alpha$  absorption coefficient and  $t$  film thickness. Figure 2-9 shows the measurement set-up used in this work. The

photodetector is placed behind the sample to measure the intensity when the sample is removed. A concave lens is used to increase the laser beam size and thus cover all of the sample and detector uniformly. Transmission is measured by calculating the transmission ratio of glass and film to glass alone. Absorption is calculated from the transmission measurement. Due to the thickness of the films probed, in this experiment reflection is assumed to be insignificant compared with the absorption.



**Figure 2-9 Steady state photoconductivity set-up used for the mobility-lifetime product measurement**

Monochromatic incident light with a wavelength of 600nm is preferred for this measurement to allow uniform absorption of the light across the film thickness [36]. However in the absence of such a light source a laser source with a wavelength of 532nm is used.

### 2.2.6 Other Experimental Methods

In addition to the core experimental set-ups mentioned earlier a number of other methods have been used for the investigation of the material and devices. The Fourier transform infrared spectroscopy was used to investigate the films molecular bonds. In this work FTIR has been used to detect the type of Si-H ( $2000\text{ cm}^{-1}$  for monohydrate and  $2090\text{ cm}^{-1}$  for dihydrides or clustered hydrogen) bonds in amorphous silicon films as well as their relative intensity [45].

The film thickness was measured using both a profilometer (Veeco Dektak 8 surface profiler) and a spectroscopic ellipsometer (Horiba MM -16 Spectroscopic Ellipsometer, 430nm to 850nm) with an appropriate material model. For the profilometer a step edge was created by dry etching a part of the sample after the deposition of the film. The profilometer measurement provides the first estimate for the film thickness measurement which can be used to help calculate the thickness from the ellipsometer data. The ellipsometer reading, which is typically within 10% of a profilometer reading, is treated as more accurate.

The ellipsometer works by measuring the reflection coefficient for monochromatic light, polarised perpendicular and parallel to the plane of incidence. These are related to the optical properties and thickness of the sample. Using a computer for fitting a suitable model, it is possible to use this method to extract the optical properties and thicknesses for thin films on substrates. In this work the Tauc-Lorentz dispersion model is used for a-Si:H samples. The Tauc-Lorentz dispersion model has been developed for amorphous thin films where the bandgap of the film is within the measurement's spectral range [46]. The "Cauchy transparent" dispersion model is used for modelling SiN films. The Cauchy model is an empirical model which it is suitable for use in transparent films in the visible range where no significant absorption takes place [47]. This makes SiN (with a bandgap in the UV range) a suitable sample for the Cauchy dispersion model. When the profilometer reading is inconsistent with the ellipsometer fitting, or a good fit ( $K^2 < 10$ ) cannot be achieved, the profilometer reading is used.

Current-voltage measurements are performed in a dark, noise shielded box connected to a Keithley 4200-SCS Semiconductor Characterisation System with pre-amplifiers. The system's electrical noise limit is in the range of 10fA. Capacitance voltage



measurements were performed in the same box using a Keithley CV meter at 100 KHz frequency. Photoconductivity measurements are performed using a light source (halogen lamp) of intensity 100mW/cm<sup>2</sup>.

## 2.3 Review of Nanocrystalline Silicon for TFTs

### 2.3.1 Transport in nanocrystalline silicon: effect of low deposition temperature

As discussed in section 1.2, nc-Si:H TFTs exhibit a good stability under electrical bias and higher field effect mobility than a-Si:H TFTs. A number of transport models have been proposed for mixed phase crystalline/amorphous silicon films. These transport models can be grouped into three broad categories.

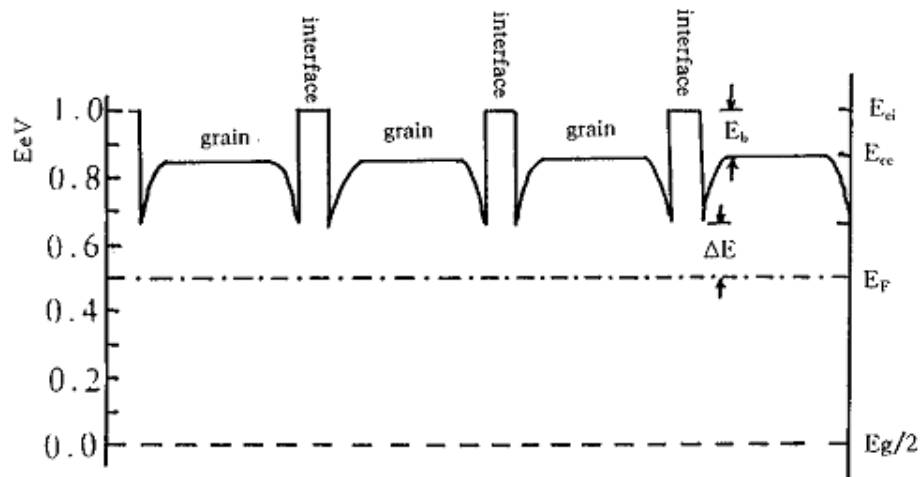
The first group includes the transport models dominated by the conduction through disordered materials where the Meyer-Neldel (M-N) rule can be observed. This rule states that the activation energy is a function of a number of factors, including bias and temperature. Therefore in the conductivity-temperature equation, shown below,  $\sigma_0$  is not constant [34].

$$\sigma = \sigma_0 \times \exp \left[ -\frac{E_A}{kT} \right] \quad (2.9)$$

The M-N rule based transport model has been reported in amorphous silicon [48], organic materials [49], and some nanocrystalline based materials [50],[51]. Typically mixed phase crystalline/amorphous films show M-N like behaviour. One can argue that this is due to having low crystal volume fractions and therefore a disorder dominant transport method [51]. However, care should be taken as such films may be produced at the early stages of crystal growth [52] and therefore are very thin films. M. Yamaguchi

and H. Fritzsche (1984) pointed out that thin amorphous silicon films would also exhibit M-N like behaviour due to their surface defects [53]. Therefore, it is unclear whether M-N like behaviour of mixed phase crystalline/amorphous films is due to disorder dominated transport or surface effects.

The second transport mechanism is the grain boundary transport (GBT) model which has been applied to nc-Si:H films [54][55][56]. Figure 2-10 shows a typical band diagram for such a model [56]. The grains are the crystalline phase and the interfaces are a-Si:H grain boundaries. The GBT model assumes ballistic transport in the grains and tunnelling through thin amorphous grain boundaries [56]. The grain boundary model is based on the approximation that defects in the material are less than the grain density, resulting in single electron ballistic transport in the grain (i.e. no diffusive transport). This model has been used to explain the capacitance-voltage and conductivity-temperature behaviour in 3~5nm grains with 50% crystallinity fraction [56].



**Figure 2-10 Band diagram for grain boundary transport model. It is assumed that the transport method in the grain is ballistic and tunnelling at the grain boundaries. Taken from [56]**

The third group of models include the unified transport models (UTM) which are based on the works of Weis (2002) [57], and Shen (2005) [58]. These models include both diffusive and ballistic transport in the grain, and tunnelling through a thin a-Si:H grain boundary. UTM has been used to explain the result of the Hall-effect mobility on thick nc-Si:H (few  $\mu\text{m}$ ) deposited on c-Si with a crystal fraction of 50% grains of about 10nm. A mobility of up to  $800 \text{ cm}^2/\text{V.s}$  has been explained using UTM [58].

Both the GBT and the UTM models predict a reduction in the mobility by increasing the donor concentration [54][58]. This can be further investigated by applying a simple approximation for a fully depleted film, with crystalline silicon grains and infinitely thin grain boundaries. The transport in the grain boundaries is assumed to be governed by thermionic emission. Figure 2-11 shows the band diagram used for this model. This transport model, or its variations, has been applied to polycrystalline silicon and has been used to explain the Hall-effect mobility vs. doping and activation energy vs. doping [55].



Figure 2-11 Band diagram for polycrystalline silicon film transport model taken from [59]

Barrier height at the grain boundary [55],  $E_b$ , is

$$E_b = \frac{qNL_G^2}{8\epsilon} \quad (2.10)$$

Where  $N$  is the density of donors and  $L_G$  is the grain size. The following equation relates the barrier height to the mobility  $\mu_{eff}$ .

$$\mu_{eff} = \frac{qV_c L_G}{kT} \exp\left(-\frac{qE_b}{kT}\right) \quad (2.11)$$

Figure 2-12 shows the effect of impurity density on the carrier mobility and barrier height for 3 different grain sizes. It suggests that lowering the impurity incorporation and using material with large grain sizes would result in higher mobility, consistent with other observed results [26]. However it should be noted that the mobilities shown in Figure 2-12 are very large. More evolved treatment of mixed phase material which accounts for the finite grain boundary has been shown to result in a lower mobility [60].

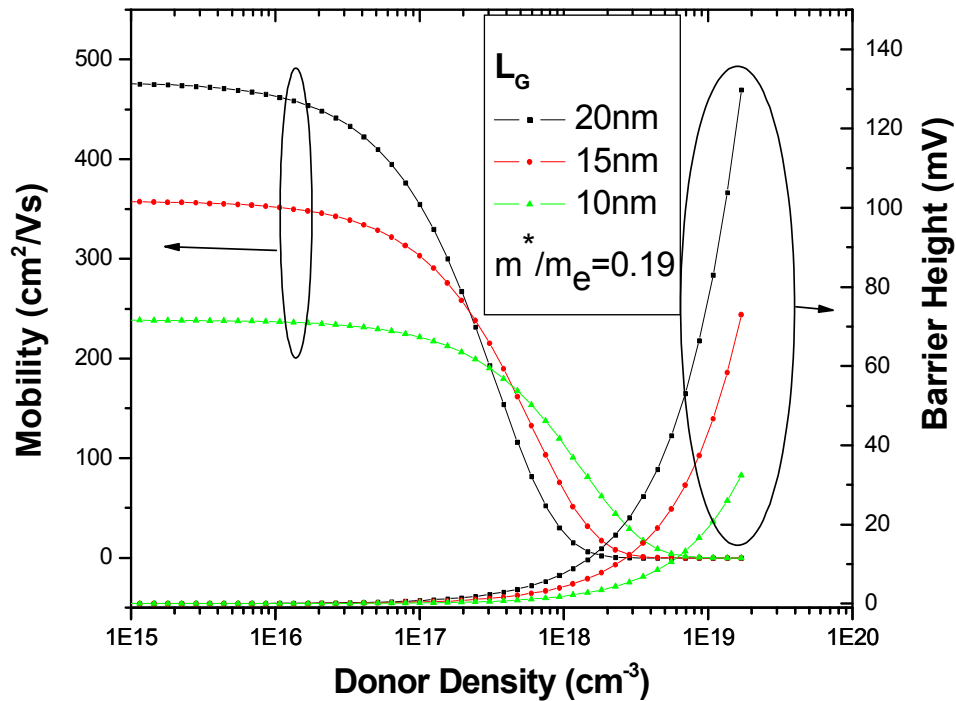
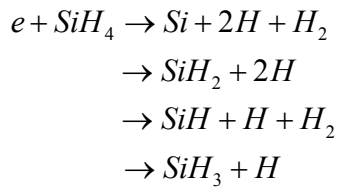


Figure 2-12 Effect of donor density on mobility and barrier height

The impurity incorporation in thin films can be intentional (i.e. doping) or unintentional. Oxygen is an example of unintentional doping due to its presence in the ambient atmosphere and it being electrically active in the silicon [61]. Secondary ion mass spectroscopy (SIMS) experiments have shown that oxygen can be incorporated in silicon thin films, even when high vacuum PECVD deposition systems are used [62]. However, it has been suggested that the density of oxygen impurities (or the density of electrically active oxygen impurities) is reduced with a reduction in the deposition temperature [62][63], leading to better quality nc-Si:H. In addition to impurities, defect states can increase the barrier height. This will be further discussed in the following section.

### 2.3.2 Nanocrystalline Silicon Growth

The deposition condition of nc-Si:H has an important effect on its properties. Therefore understanding and controlling nc-Si:H growth can lead to higher quality films and improved device performance. SiH<sub>4</sub> has generally been used as the silicon precursor in CVD growth. The following shows a few of the primary reactions which can take place [64]:



SiH<sub>2</sub> and SiH<sub>3</sub> have been shown to be the dominant species in the plasma during the a-Si:H growth [65]. The primary reactant species then move to form secondary reactions. For example secondary reactions of SiH<sub>2</sub> have been observed which result in the formation of Si<sub>2</sub>H<sub>6</sub> and Si<sub>3</sub>H<sub>8</sub> [65]. In addition to the gas phase chemistry, surface reactions influence the properties of the film. nc-Si:H has been grown at substrate

temperatures of 150 °C and lower [62][63]. These temperatures are significantly lower than the melting point of silicon and thus there is no thermal crystallisation at such a low temperature [66]. Three groups of mechanisms have been proposed for crystal formation in mixed phase crystalline/amorphous films using CVD [67]. All of these growth mechanisms may be present but some may be more dominant at certain growth phases, or deposition conditions.

The first group of models is based on hydrogen etching first proposed by Veprek *et al.* (1982) [68]. The etching model is based on the concept of preferential etching of weak silicon-silicon bonds (amorphous phase) by hydrogen ions, resulting in a higher relative growth rate of stronger silicon-silicon bonds (crystalline phase). Figure 2-13 shows the basic concept of the hydrogen etching model. This model can explain the increase in the crystal volume fraction with an increase in hydrogen dilution, as well as the sharp reduction in the growth rate with hydrogen dilution at very high dilutions, as shown in Figure 2-14 [67]. However, for nc-Si:H deposition at low hydrogen dilutions this model fails to account for the linear relation between deposition rate and  $\text{SiH}_3$  radicals (the main silicon precursor in CVD). Furthermore, it fails to establish a link for reduction in crystal fraction with increasing deposition temperature [69].

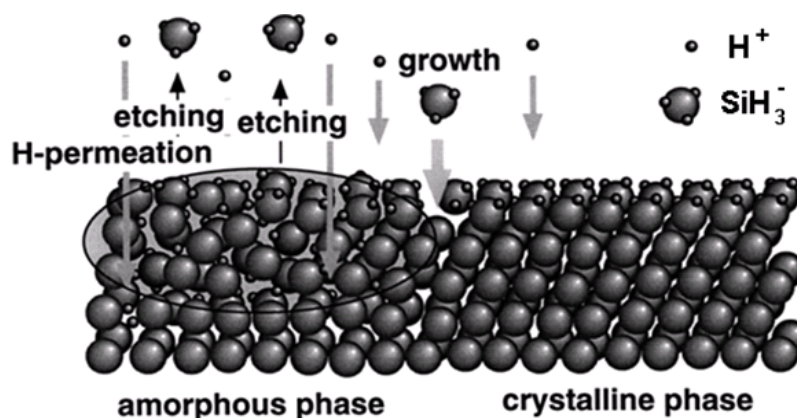


Figure 2-13 Hydrogen etching model taken from [67]

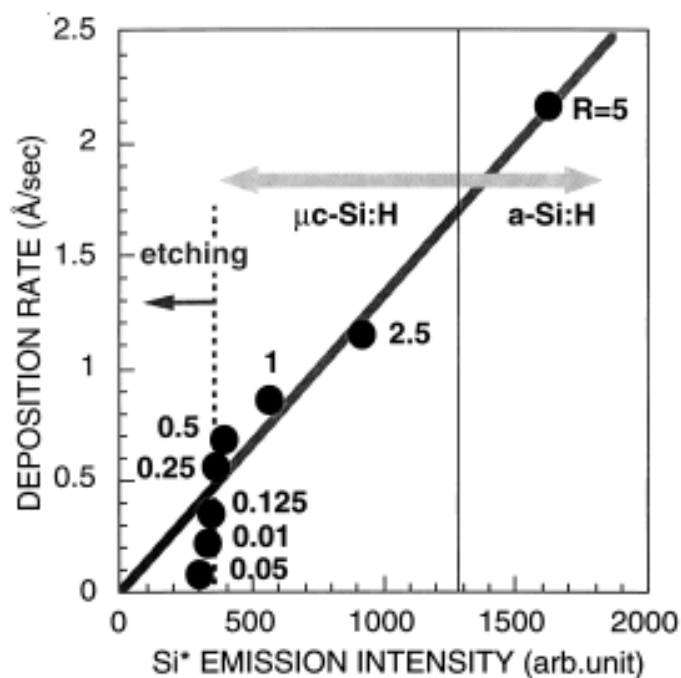
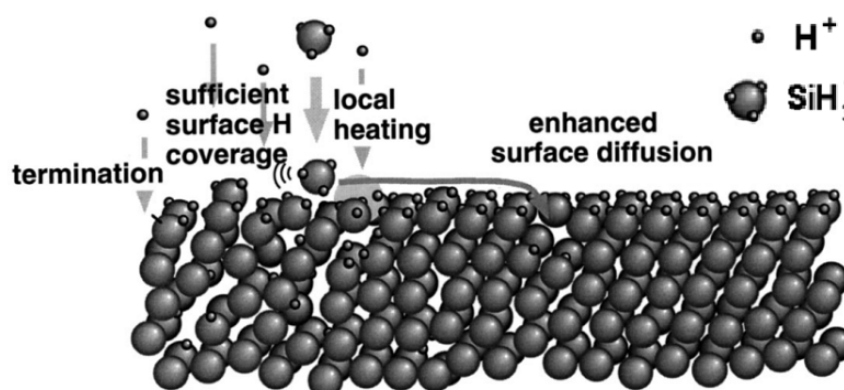


Figure 2-14 Effect of silicon precursor on deposition rate. R is the  $[\text{SiH}_4]/\text{H}_2$ . Taken from [67]

The second mechanism is the surface diffusion model. This mechanism is based on the idea that  $\text{SiH}_3$  radicals are mobile on the film surface enabling them to move to sites with favourable energies. During the growth,  $\text{SiH}_3$  is weakly adsorbed by hydrogen-covered surface [67]. The weak adsorption combined with local heating from two hydrogen recombination (exothermic recombination) results in high surface mobility of  $\text{SiH}_3$  radicals and long surface diffusion lengths [69]. Initially, this results in a smoothing effect which has been observed using real time spectroscopic ellipsometry at the nucleation stage of nanocrystalline silicon [70]. As the crystalline phase continues to grow with time, epitaxial like crystal growth takes place, resulting in surface roughening. Figure 2-15 shows the concept of surface diffusion model.



**Figure 2-15 Precursor surface diffusion model taken from [67]**

This model can account for the peak in the crystal fraction as a function of deposition temperature [67]. It can be used to explain the results of experiments showing that the continuous flow of hydrogen is not required for growth of nc-Si:H [71]. This model also accounts for the advantage of using chlorine-terminated surfaces [72].

However, the surface diffusion model fails to recognise that there cannot be one continuous phase of crystalline growth during the deposition [69] and that nc-Si:H growth is typically a two phase process. Furthermore, it is thought that during the deposition of a-Si:H, the surface of the film is already fully passivated with hydrogen, therefore the role of further hydrogen for crystal formation is not clear.

The third proposed crystal growth mechanism is the solid phase crystallisation model, assisted by chemical annealing. It describes the sub-surface transformation of the amorphous phase to the crystalline phase [73]. This model is based on the idea of permutation by hydrogen atoms in the a-Si:H film. This allows the a-Si:H network to change its bonding configuration to a lower energy state, resulting in relaxation of the amorphous structure and crystallisation of a-Si:H. This process is further enhanced by the exothermic reaction of Si-H abstraction by atomic hydrogen in the subsurface [69]. Figure 2-16 summarises the concept of the solid phase transformation model.



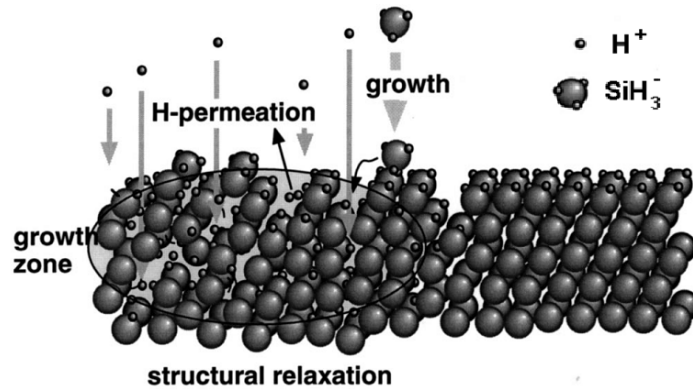


Figure 2-16 Chemical annealing is a solid phase [67]

There is some evidence for solid phase transformation [74] but it is not conclusive as shown by Matsuda (1999) who suggested that the layer-by-layer deposition method does not result in crystalline phase formation if the substrate is shielded [67].

These growth mechanisms provide an explanation for nc-Si:H growth using PECVD, but none of them explains the nc-Si:H growth from the thermodynamic perspective. This was first introduced by J. Robertson (2003) [69]. Although his thermodynamic model does not conclusively rule out any of physical models of crystal formation in the CVD method, it does provide a useful explanation for the relation between nucleation rate, crystal volume fraction, deposition temperature, and hydrogen dilution. From the thermodynamic perspective the total energy gain from the nucleation is the sum of surface energy (positive) and volume energy (negative). This results in a favourable critical nucleation size,  $r^*$ , where the energy gain  $\Delta G^*$  is maximum as shown in Figure 2-17. The following equation relates the energy term to a critical size [69]:

$$r^* = \frac{2\gamma}{\Delta G_v} \quad \text{where} \quad \Delta G_v = \frac{L}{T_x(T_x - T)} \quad (2.12)$$

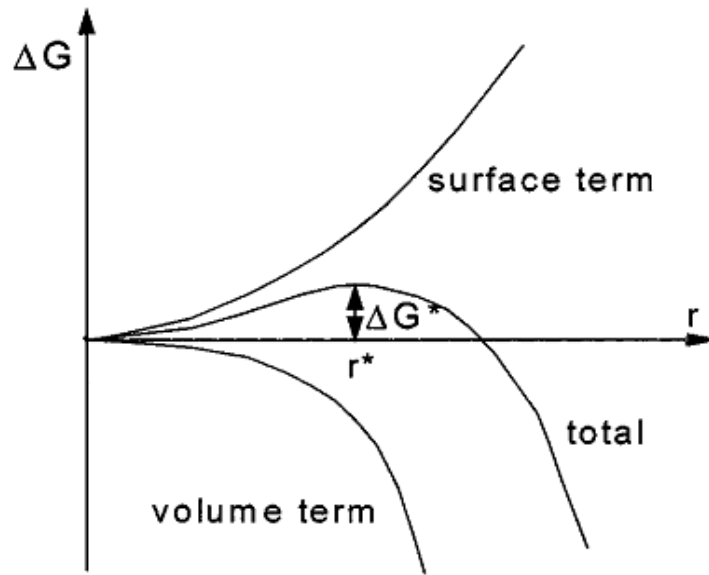


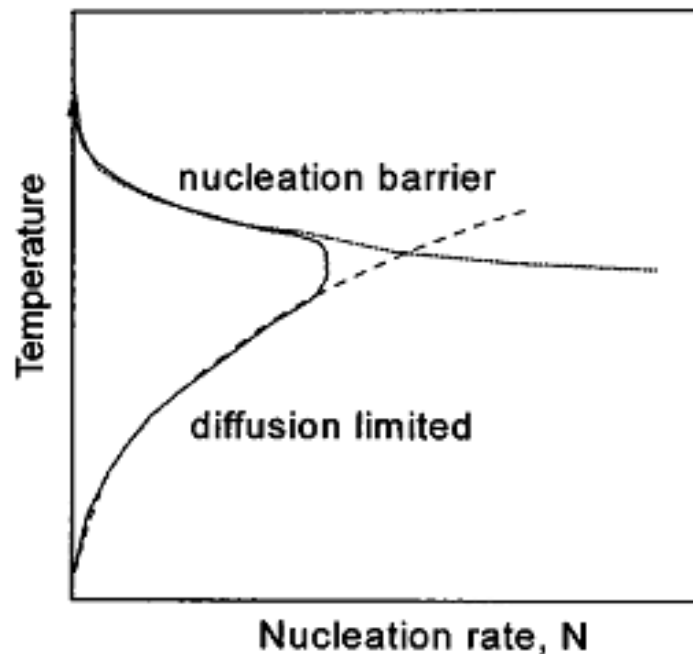
Figure 2-17 The energy gain (positive) as a function of nuclear size take from [69]

$T_x$  is the approximate crystallisation temperature of unstrained amorphous silicon (650°C and lower for strained network) and  $T$  is the deposition temperature. Therefore the critical nucleation size,  $r^*$  for the following dependence of deposition on temperature.

$$r^* \propto \frac{1}{(T_x - T)} \quad (2.13)$$

This shows that a reduction in the deposition temperature results in a reduction in the crystal size. This reduction in the temperature would be accompanied by a reduction in the nucleation rate, leading to a low crystal fraction. However, given that deposition temperatures for the nc-Si:H are much lower than  $T_x$ , this reduction will not be substantial, and other factors may influence the growth further at lower temperatures. Figure 2-18 shows the effect of deposition temperature on the nucleation rate. It can be seen that at lower temperatures the nucleation rate is limited by the diffusion of the precursors. Therefore, the limited nucleation effect can be compensated by increasing

the hydrogen dilution at the expense of lower growth rate, as the etching growth mechanism may dominate.



**Figure 2-18** The nucleation rate as a function of temperature taken from [69]

As discussed in the previous section deposition of intrinsic nc-Si:H at low temperatures has an important advantage. The relation between carrier density and deposition temperature in an nc-Si:H film is shown in Figure 2-19. It can be seen that low deposition temperature results in a lower density of carriers. This is desirable as it results in lower grain boundary barrier height, leading to high mobility nanocrystalline silicon as discussed in the section 2.3.1.

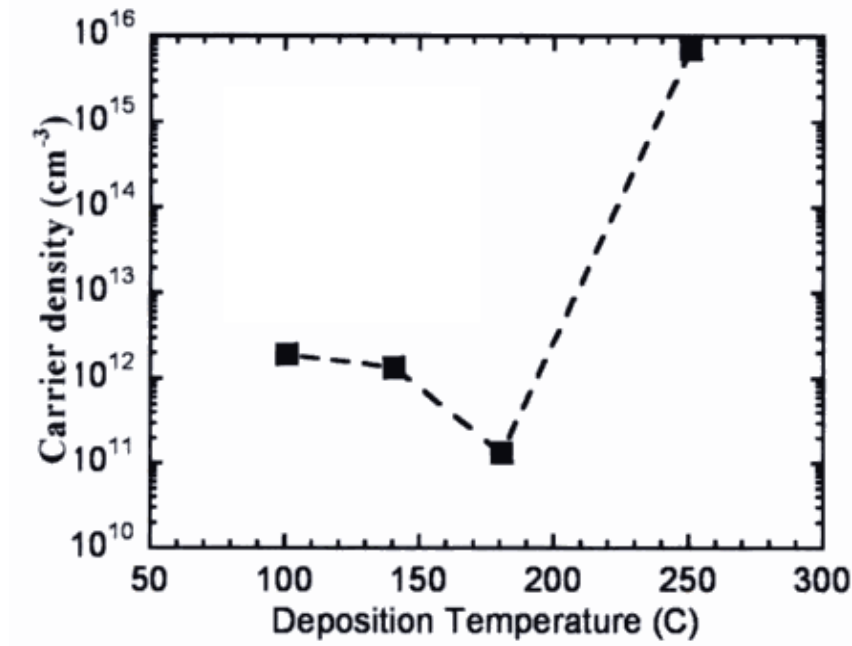


Figure 2-19 Oxygen related carrier density as a function of deposition temperature [75]

As well as grain size and density in nc-Si:H, the defect density must be considered and controlled. One possible location of defects is at the a-Si:H grain boundary. There is a link between the deposition rate, pressure and the deep defect density as measured by electron spin resonance (ESR) for a-Si:H. As Figure 2-20 suggests, higher deposition pressure and lower power (and therefore lower deposition time) results in lower defect density. Although Figure 2-20 is for a-Si:H growth, given that nanocrystalline silicon would have an amorphous silicon tissue, a high-pressure and low-power approach may be beneficial for obtaining high quality material. Therefore a lower power and higher pressure deposition condition is desirable. Furthermore, as discussed in section 2.1, higher pressure would result in a more uniform deposition at a high gas flow rate.

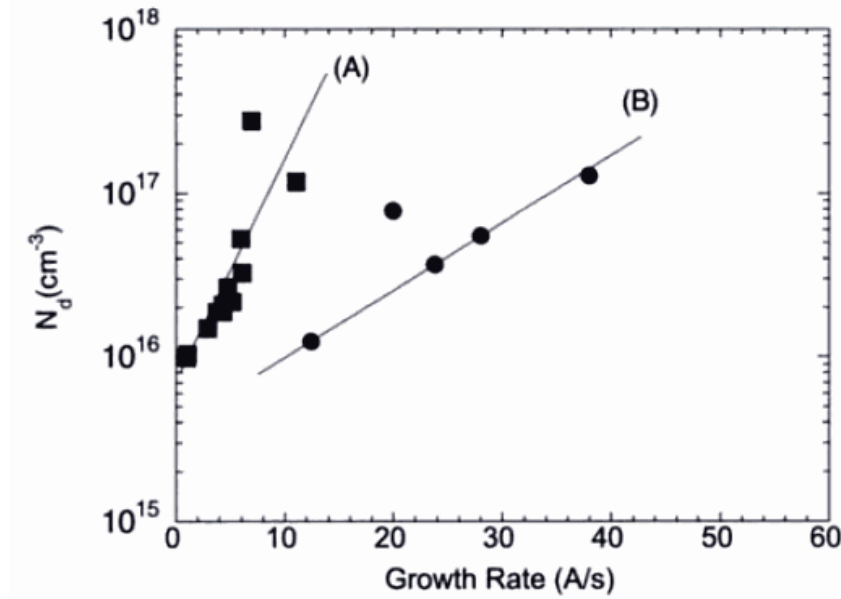


Figure 2-20 Effect of pressure on ESR defect density as a function of growth rate taken from [76]

Low temperature growth of amorphous silicon results in dihydride and polyhydride formation in the amorphous silicon [45]. It is known that adding hydrogen results in lower hydrogen incorporation in amorphous silicon by the process of hydrogen abstraction [77]. However, some theoretical work suggests that this process is inefficient at lower temperatures [77] and adding helium may have some benefit [78].

## 2.4 TFT Material Optimisation

### 2.4.1 Intrinsic Layer

The films are deposited at a power density of  $21.5 \text{ mW/cm}^2$  and pressure of 0.8 Torr on glass substrate (Corning Eagle 2000). A relatively high pressure is used to minimise the pressure variation across the chamber at the high gas flow rates (needed for high  $\text{H}_2$  dilution). In section 2.1.1 the stability of the plasma voltage was investigated and it was concluded that low power growth is more suitable for the PECVD system. Although the power density used in this work is lower than the one generally used for the deposition

of nanocrystalline silicon [62], it is selected for better plasma stability and lower defects. Low temperature growth can lead to a large concentration of dihydrides in the silicon film. It has been shown that the addition of helium may reduce the hydrogen concentration in the a-Si:H thin film without the introduction of defect states by the process of soft ion bombardment [79].<sup>5</sup> Table 2-1 shows the deposition parameters used in this work. In this work helium, hydrogen and SiH<sub>4</sub> were used for the growth of a suitable intrinsic nc-Si:H. The effect of silane dilution, as well as He to H<sub>2</sub> ratio, was investigated.

<i>Sample Number</i>	<i>SiH<sub>4</sub> Flow Rate (SCCM)</i>	<i>H<sub>2</sub> Flow Rate (SCCM)</i>	<i>He Flow Rate (SCCM)</i>	<i>Deposition Pressure (Torr)</i>	<i>Substrate Temp (C)</i>	<i>Power (W)</i>
1	2	100	100	0.8	150	5
2	2	50	50	0.8	150	5
3	2	25	25	0.8	150	5
4	2	10	10	0.8	150	5
5	2	50	150	0.8	150	5
6	2	25	75	0.8	150	5
7	2	12	36	0.8	150	5
8	2	5	15	0.8	150	5
9	2	150	50	0.8	150	5
10	2	75	25	0.8	150	5
11	2	36	12	0.8	150	5
12	2	15	5	0.8	150	5

**Table 2-1 Deposition parameter used for the nc-Si:H investigation**

<sup>5</sup> It should be noted that his work was done using electron cyclotron resonance (ECR) plasma deposition. ECR deposition results in a higher density, lower energy plasma species. Therefore the results are not directly applicable to this PECVD deposition.

Figure 2-21 shows film growth rate as a function of the  $\text{SiH}_4$  dilution ( $[\text{SiH}_4]/[\text{H}_2]+[\text{He}]$ ) for three different helium to hydrogen ratios. It can be seen that the growth rate decreases as silane dilution is reduced. Furthermore, it can be seen that a higher ratio of helium to hydrogen results in a higher growth rate. This can be due to the higher disassociation rate of silane in the presence of helium plasma [80]. Some non-linearity can be observed for samples with high  $\text{H}_2$  ratio and low silane dilution, indicating a preferential etching growth mechanism.

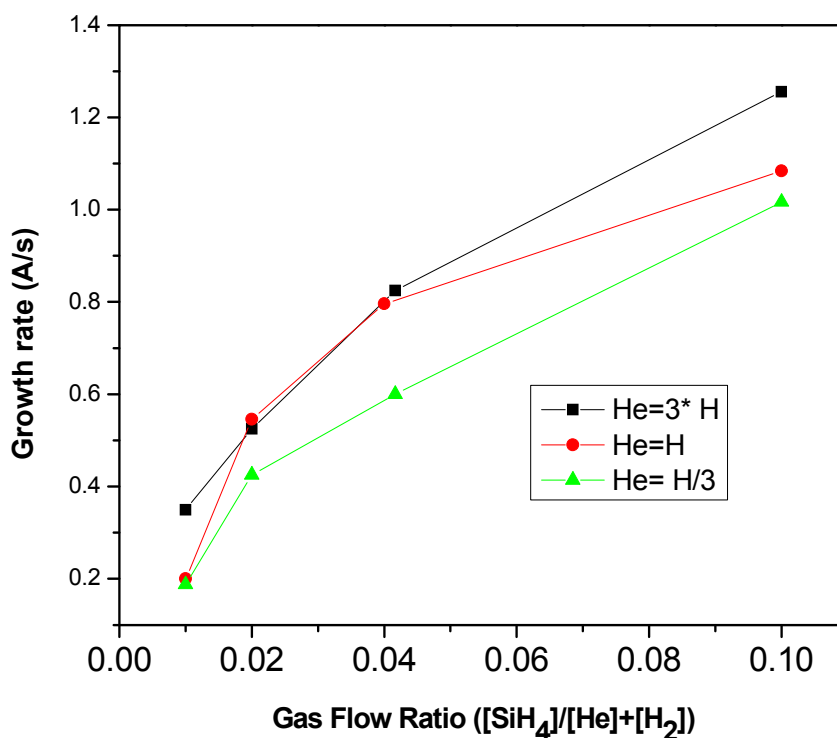
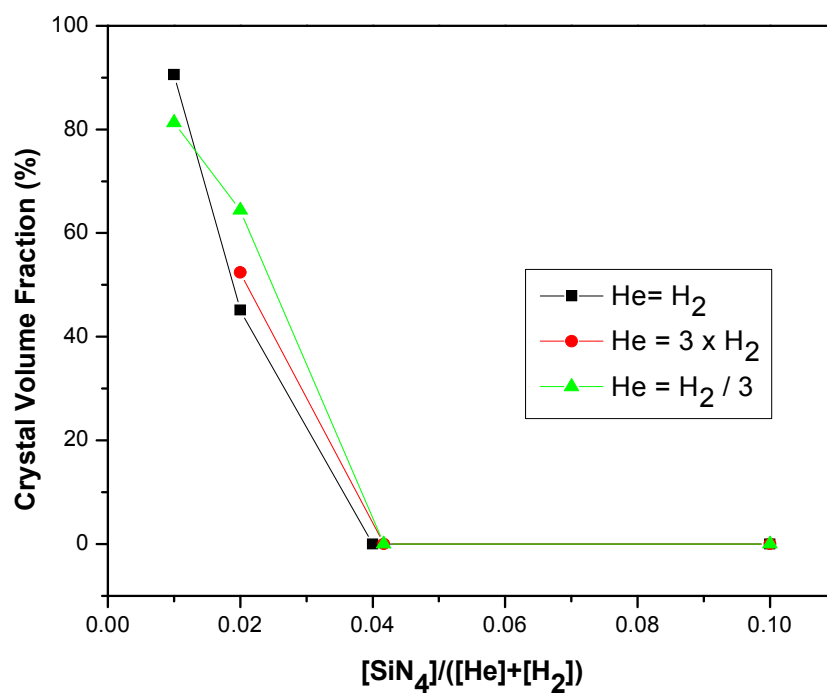


Figure 2-21 Growth rate as a function of silane dilution

Figure 2-22 shows the crystal volume fraction as a function of silane dilution. Low silane dilution results in higher crystalline volume fraction. The effect of He to  $\text{H}_2$  ratio on crystal volume fraction is inconclusive due to the inherent error when using Raman

spectroscopy.



**Figure 2-22 Crystal volume fraction as a function of silane dilution**

Figure 2-23 compares the Raman scattering peak location of samples 1 and 9; two of the samples with high crystal volume fraction. It suggests that sample 9, with a peak location of  $520\text{cm}^{-1}$ , contains larger crystals (or less stress) than sample 1, with a peak location of  $517\text{cm}^{-1}$ .



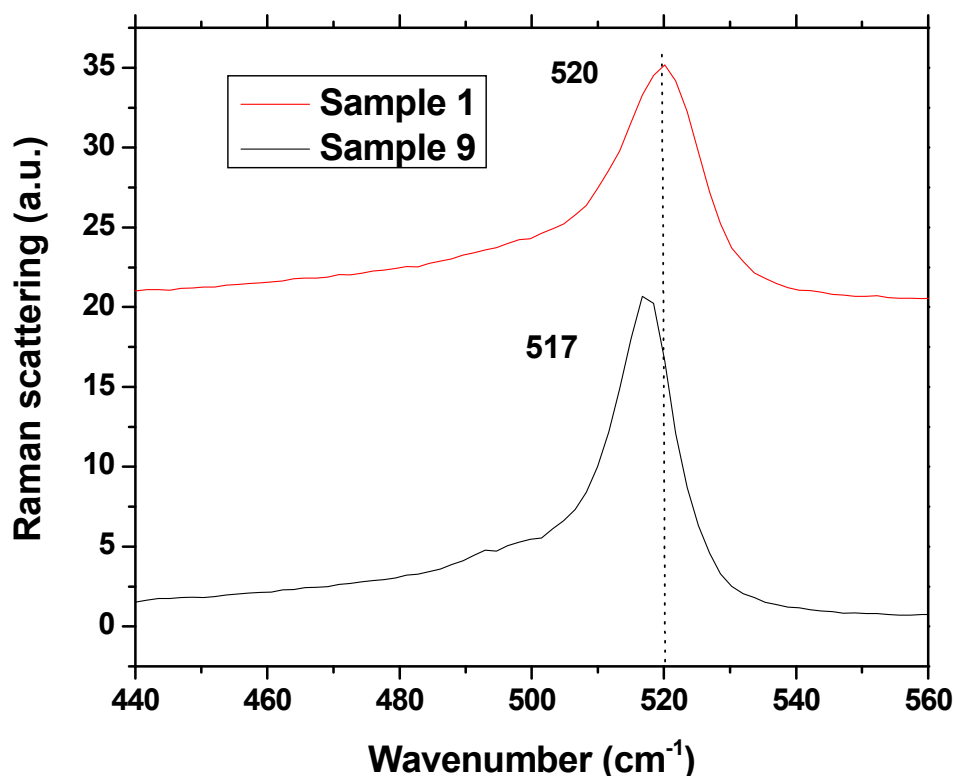
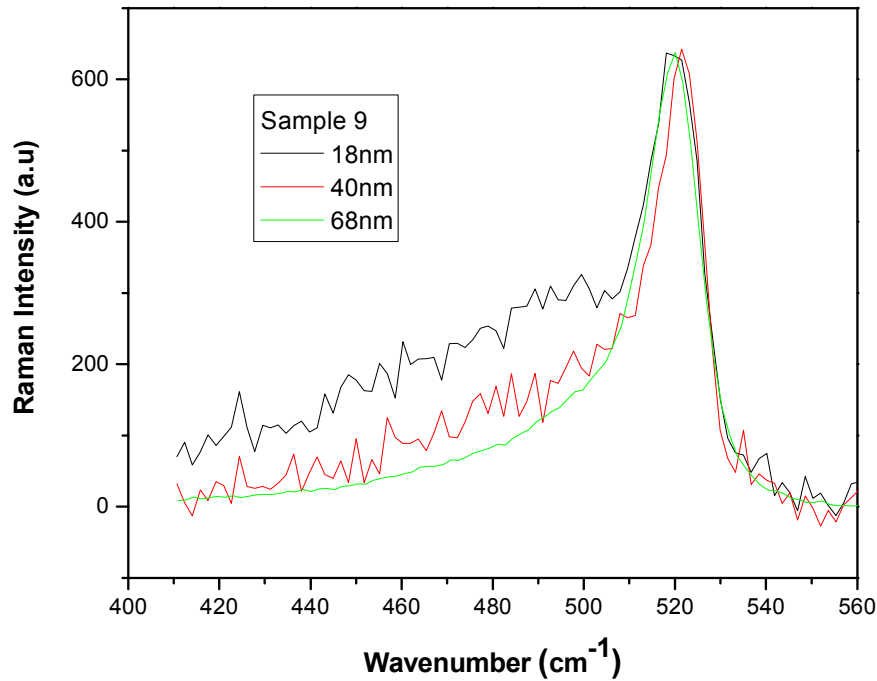


Figure 2-23 Raman spectra of two samples with high crystal volume fraction

It is important to investigate the evolution of nanocrystalline film with thickness. For this two further samples with thicknesses of 18nm and 40nm were deposited. The growth rate for all 3 films is approximately constant (1.2nm/min for a 18nm film, 1.3nm/min for a 56nm film and 1.1nm/min for a 68nm film). Figure 2-24 shows the changes in the Raman spectra with thickness. The 18nm sample has some crystalline phase (36% crystalline volume fraction), pointing to a thin incubation layer. As expected, with an increase of film thickness the volume fraction increases (56% for the 38nm film and 80% for the 68nm film). A thin incubation layer is desirable from a TFT application perspective as it results in higher mobility and better device stability.



**Figure 2-24 Raman Spectra of different film thicknesses using sample 9 deposition conditions**

Samples 1 and 9 have relatively high dark conductivities of  $4.2\text{E-}4$  S/cm and  $7.6\text{E-}6$  S/cm respectively. High dark conductivity ( $10^{-3}$  s/cm) has also been observed for nc-Si:H samples using He only dilution [81]. The high value of the dark conductivity can be due to low activation energy. Two factors may affect the activation energy: grain boundary trap density or grain size [82]. High defect density in the grain boundary results in a low activation energy, higher dark conductivity and lower mobility [83]. Furthermore, using samples with high dark conductivity may result in lower on/off ratio transistors. Intrinsic mc-Si used in solar cell devices with over 90% crystal volume fraction and activation energy of 0.5~0.6eV have a dark conductivity of  $1.5\text{E-}7$  S/cm [36], lower than both samples 1 and 9. High mobility nc-Si:H TFTs with dark conductivity of  $\sim 1\text{E-}6$  S/cm have been reported [26]. Sample 9 appears to be closer to this value, and therefore more suitable for device application.

In this section a growth condition has been identified which leads to a good quality nc-Si:H film on glass substrate. It should be noted that a growth of nc-Si:H is highly substrate dependent, and ultimately the quality of nc-Si:H as grown on the gate dielectric would influence the TFT properties.

### 2.4.2 Silicon Nitride

In this work higher plasma power is used for the growth of silicon nitride when compared with a-Si:H or nc-Si:H. However, as explained in section 2.1, higher plasma power leads to instability in the PECVD, and poor film uniformity (non-centric). For this reason pulsed-RF power was used, as it appeared to offer higher plasma voltage stability and better film uniformity at higher powers in the PECVD system used. Plasma power of 30W (200Hz and 50% duty cycle), a pressure of 0.8 Torr, and a substrate temperature of 150°C was used. The precursor gas ratio of  $\text{SiH}_4/\text{NH}_3 = [4]/[40]$  sccm was diluted in 120 sccm  $\text{H}_2$ . The  $\text{SiH}_4/\text{NH}_3$  gas flow ratio was selected in line with other works [84][85].

Figure 2-25 shows the FTIR spectrum of the silicon nitride film deposited. As expected for a silicon nitride deposited at a low temperature [85], this film contains significant N-H and Si-N bonds. This film also shows a significant Si-H<sub>n</sub> bonding. The ratio of the Si/N as well as the hydrogen content of silicon nitride has been extracted using FTIR [86]. However, this approach does not yield consistent results with elemental analysis methods such as elastic recoil detection [87], and therefore it was not explored. The FTIR spectrum suggests the presence of some Si-H bonds. This may suggest that the film is not a nitrogen-rich film. This could lead to higher charge trapping and subsequent device instability [85][17]. The device instability using silicon nitride will be investigated in section 3.4.4.

It is possible to achieve nitrogen-rich samples by optimising the  $\text{SiH}_4/\text{NH}_3$  gas ratio. However this was avoided in this work, in order to investigate the effect of device instability on the circuit performance.

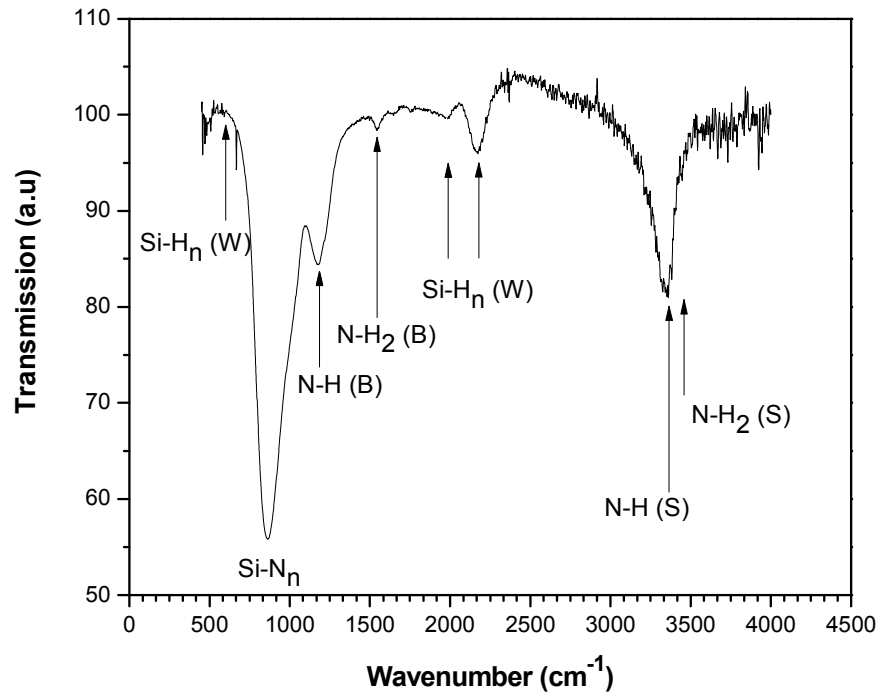


Figure 2-25 FTIR spectrum of  $\text{SiN:H}_x$ . Location of the peaks are taken from [88]

For the electrical characterisation  $\text{SiN:H}$  was deposited on a degenerately p-type c-Si substrate. First a solvent cleaning step was performed. Before loading in the PECVD, the native oxide was etched using buffered HF etch, rinsed in DI water bath to a resistivity of  $11\text{M}\Omega$ , and dried using a nitrogen gun. The time lapse between the removal from the buffered HF bath and loading into the PECVD was less than 2 mins. A thermal evaporator was used for the deposition of the chromium (100nm) contact. Using a shadow mask with various square sizes different size test structures were fabricated. A growth rate of 0.8 Å/s and uniformity of 8% over 2.5" diameter on 3" wafers were achieved, measured by using an ellipsometer. A breakdown field

measurement was performed by applying a voltage sweep of 0 to 100V (substrate grounded) with a ramp rate of approximately 2V/s, leading to a measurement time of approximately 40s to 50s. The leakage current was monitored during the measurement. Breakdown was defined as hard-breakdown and easily identified from the current-voltage graph.

Figure 2-26 shows the distribution of the breakdown field of a 150nm SiN:H film for different electrode sizes. The median breakdown field for pulsed-RF samples for all sizes is between 4 and 5 MV/cm. In device applications, typically an SiN:H film thickness of 250~300nm is used. The breakdown field is expected increase with the increase in the film thickness [84].

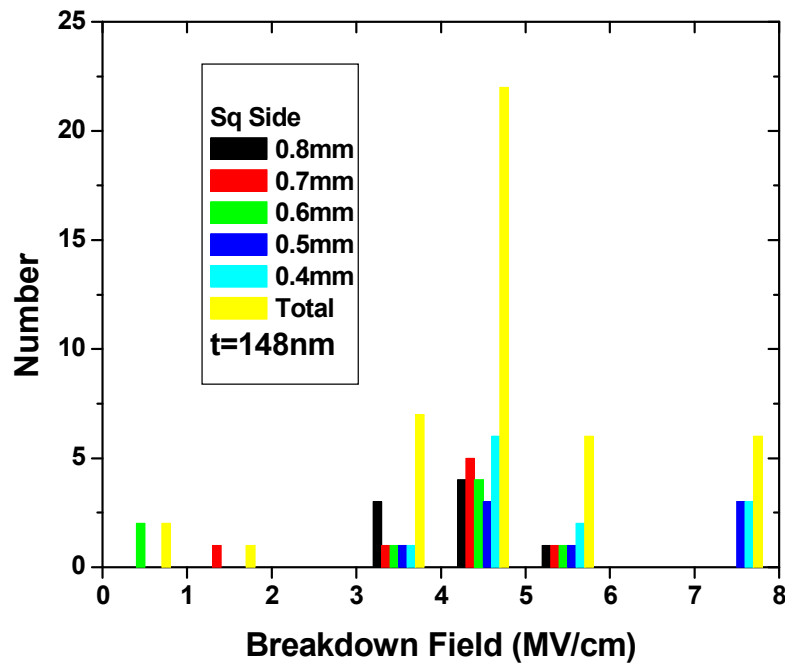


Figure 2-26 Breakdown field as a function of MIS area

A correlation between high hydrogen content and high HF etch rate has been shown [89]. Also conceptually, high void density and porosity can be related to high etch rate.

From a device perspective, it is important to establish whether high etch rate is due to hydrogen content, porosity, or both. The density was calculated by weighing the substrate before and after film deposition, and assuming uniform deposition. The value for the SiN:H film was calculated as  $2.8\text{g/cm}^3$ . The relative dielectric constant of 6.06 at 1MHz was extracted from the capacitance voltage measurement. These and the breakdown field distribution (same median range across all sizes) suggest that the film does not contain a high density of voids and therefore is suitable for device application. However, the high etch rate would make the device fabrication complicated.

Table 2-2 compares some of the properties of the SiN:H used in this work with that used in other work. It can be seen that the SiN:H film has a low breakdown field and low leakage when compared with other work. However, as discussed, the breakdown field and leakage are both thickness dependent. Therefore the breakdown field and resistivity will both increase further when a 300nm film is used. The density of the film produced here appears to be higher than other film densities. However the density measurement method used in this work has a degree of error, and therefore this comparison maybe inconclusive. One alternative density measurement method involves measurement of the x-ray's critical angle of reflection [90]. This can be used to confirm the validity of the comparison.

	<i>SiN:H</i> <i>120°C [85]</i>	<i>260°C</i> <i>PECVD[91]</i>	<i>Pulsed SiN:H</i> <i>150nm, 150°C</i>
<i>Breakdown Field</i> <i>(MV/m)</i>	5.5	8	4.5
<i>Resistivity (Ohms-cm)</i> <i>(@ 1MV/cm)</i>	$2 \times 10^{15}$	$10^{15}$	$3 \times 10^{14}$
<i>Relative permittivity</i>	6.2	6.5	6.1
<i>Mass density (g/cm<sup>3</sup>)</i>	2.1	2.7	2.8

**Table 2-2 Properties of SiN:H used in this work compared with the other PECVD SiN:H in other works**

### 2.4.3 N-Type Nanocrystalline Silicon

N-type nanocrystalline silicon was used for the contact layer. For the a-Si:H channel layer a seed layer (SL) was deposited on the intrinsic amorphous silicon layer (5nm) before the growth of the nanocrystalline silicon. The SL was grown at 150°C with 5W power at 0.8Torr using silane (2sccm) and 1% PH<sub>3</sub> (1sccm) and H<sub>2</sub> (300sccm). The nanocrystalline silicon was grown using lower power (2W), lower H<sub>2</sub> flow rate (200sccm) and higher PH<sub>3</sub> flow rate (2sccm).

Figure 2-27 shows the evolution in crystallinity as a function of film thickness. An 8nm i-layer is deposited on glass to emulate the surface of the i-layer. The thickness of the SL is 3~5nm and no c-Si signal is detected in the Raman. However this does not indicate the absence of crystalline formation: 5nm is too thin to exhibit a significant Raman signal especially when the SL is deposited on an a-Si:H film. After 5nm growth of nc-Si:H, a crystalline peak can be observed.

A 40nm film was used in this work. n-type nc-Si:H exhibited a low resistivity of 0.25 S/cm. In calculating the resistivity, the contribution of the a-Si:H and the seed-layer was neglected. The resistivity is consistent with the n+ nc-Si:H, used in other work for TFT applications [92].

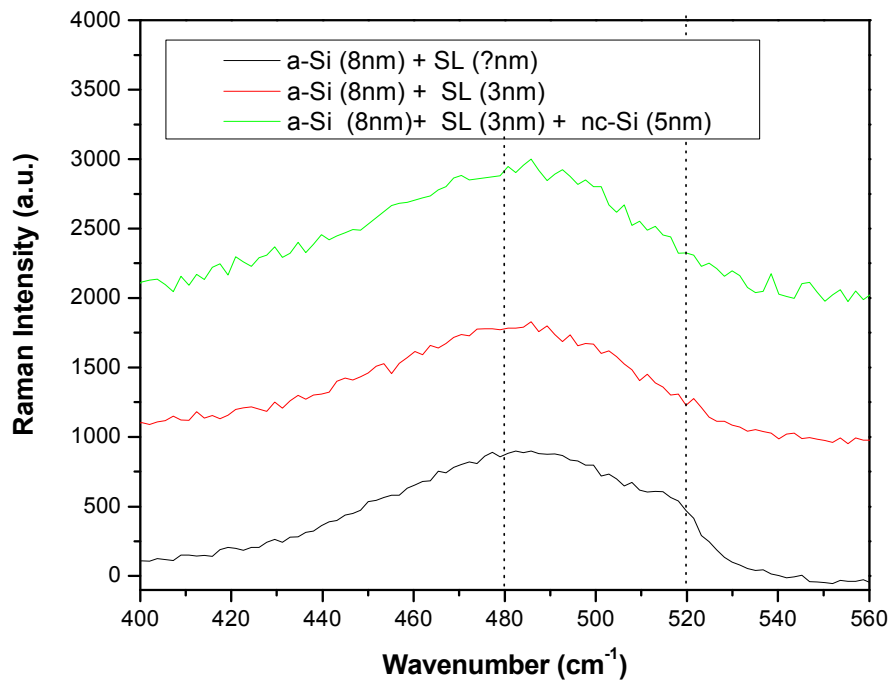


Figure 2-27 Raman spectra of early stages of n-type nc-Si:H growth

## 2.5 Review of Solar cell material requirements

The sheet resistance required for the front contact of the solar cell should be better than  $10 \text{ } \Omega/\text{Sq}$  [36]. Standard ITO (Indium-Tin-Oxide) coated glass satisfies this requirement. Table 2-3 summarises the material requirements for the i, p and n-type a-Si:H when used in the solar cell.

Layer	Property	Value
Intrinsic	Dark Conductivity	Less than $1\text{E-}10 \text{ /ohm.cm}$
	Photoconductivity	More than $1\text{E-}5 \text{ /ohm.cm}$
	Tauc Bandgap	Less than 1.8ev
P-type	Conductivity	More than $1\text{E-}5 \text{ /ohm.cm}$
	Bandgap	More than 2.0ev
N-type	Conductivity	More than $1\text{E-}3 \text{ /ohm.cm}$

Table 2-3 Basic electrical and optical properties of i, p and n-layers. Taken from [36]



### 2.5.1 P-Layer Selection

The window layer needs to be wideband p-type and conductive. Films such as a-SiC:H, nc-Si:H and a-SiN:H<sub>x</sub> have been used to create wideband p-layers. Although a-Si:H:N<sub>x</sub> would result in a wide bandgap, it has a low conductivity and has not been widely used [21]. a-SiC:H and nc-Si:H are two of the most widely used, with the latter one often being used for the *substrate structures* (n-i-p). The use of a-SiC:H in *substrate structures* results in poor p/i interface and low Voc[93]. *Substrate structures* using p-type nc-Si:H and appropriate hydrogen plasma treatment at the p/i interface result in Voc=1V [94]. Small grain (less than ~5nm) n-Si:H films show a quantum size effect leading to a wide bandgap of around 2ev. Furthermore, it has been shown that small grain nc-Si:H results in a larger Voc and higher efficiency [94]. Table 2-4 summarises the requirements for the p-type nc-Si:H.

	P-type nc-Si:H
<b>Band gap (ev)</b>	2
<b>Conductivity (S/cm)</b>	1E-2
<b>Voc (V)</b>	Close to 1V using p-i interface
<b>Isc (ma/cm<sup>2</sup>)</b>	10
<b>Fill Factor (%)</b>	69
<b>Efficiency (%)</b>	5.7~7.2

**Table 2-4 Properties of nc-Si:H p-layer and the associated solar cell properties. Taken from [95]**

In the superstrate structure, the use of p-type a-SiC:H is more commonly used as it allows a better control of the p-i interface using a graded layer (GL), and thus avoids the sharp transition between p-type nc-Si:H and a-Si:H. Table 2-5 summarises the typical properties of p-type a-SiC:H and properties of the highest efficiency superstrate structure achieved.

	<b>P-type a-siC:H</b>
<b>Band gap (ev)</b>	More than 2
<b>Conductivity (S/cm)</b>	More than 1E-6
<b>Voc (V)</b>	0.86V using optimised p-i interface
<b>Isc (ma/cm2)</b>	18.7 (with anti-reflective coating)
<b>Fill Factor (%)</b>	63
<b>Efficiency (%)</b>	9.47%

**Table 2-5 Properties of a-siC:H p-layer and state of the art solar cell properties. Taken from [96]**

Comparing Table 2-5 and Table 2-4 shows that the conductivity of the p-type a-SiC:H is significantly lower than p-type nc-Si:H. However, as discussed in 2.2.2 this conclusion may be unreliable. Furthermore, the main role of the p-layers (in conjunction with the other layers) is to provide the built-in electric field, and the charge would only travel through a thin p-layer (typically less than 20nm) before reaching the TCO (transparent conducting oxide) electrode. The conductivity of the film is an indicator of the film's activation energy, which is critical to the device performance. Therefore, the contribution of the p-layer resistivity to the series resistance would be small. The unreliability of the conductivity measurement, and/or the insignificance of the conductivity are demonstrated by the similarity of the FF achieved when using superstrate and substrate structures. In this work p-type a-SiC:H will be used.

## 2.6 Solar cell Material Optimisation

### 2.6.1 Intrinsic Layer

It is known that low temperature growth of amorphous silicon leads to the incorporation of di and poly-hydrides. A number of methods have been proposed to eliminate this problem. It has been suggested that reducing the gas residence time in the PECVD may partially eliminate this problem [45]. An alternative method of hydrogen

abstraction, by adding additional  $H_2$ , has also been suggested [77]. In addition to these methods the effect of He ion bombardment on hydrogen abstraction and film properties has been investigated. Helium dilution has already been used for a-Si:H deposition [97][98]. It has been shown that high deposition pressure, high RF power and helium dilution (in place of hydrogen) results in a higher deposition rate. Film quality similar to  $H_2$  dilution can be achieved after post deposition annealing (175°C for 30min) [97]. However in this work annealing at 175°C is not acceptable, and the effect of combined He and  $H_2$  is investigated.

Five samples have been prepared in this work, as outlined in Table 2-6. Samples 1 and 4 are grown using undiluted silane. Sample 2 has high  $H_2$  dilution and Sample 3 has high He dilution. Samples 2, 3, and 4 have the same gas residence time. Commonly  $SiH_4$  is diluted with  $H_2$  only. This approach was tested for sample 5.

Sample Number	$SiH_4$ Flow Rate (SCCM)	$H_2$ Flow Rate (SCCM)	He Flow Rate (SCCM)	Deposition Pressure (Torr)	Substrate Temp (°C)	Power (W)
1	6	0	0	0.8	150	5
2	2	5	15	0.8	150	5
3	2	15	5	0.8	150	5
4	22	0	0	0.8	150	5
5	2	20	0	0.8	150	5

**Table 2-6 a-Si:H deposition condition**

Figure 2-28 shows the FTIR spectrum of amorphous silicon films. Samples 1 and 4 exhibit peaks at around  $880cm^{-1}$ ,  $907cm^{-1}$ , and  $2090cm^{-1}$  indicating the presence of di and poly-hydrides [45]. Comparing samples 1 and 4 suggests that at 150°C, simply reducing the silane residence time does not eliminate the formation of dihydrides and polyhydrides. However, diluted samples (2 and 3) show a significant reduction in the di and poly-hydrides peaks.

An approximate hydrogen content can be determined from the area under the wagging mode vibration peaks at 630~640  $\text{cm}^{-1}$  [36]. Assuming the same film thickness, the relative area under 630~640  $\text{cm}^{-1}$  can be used as an indicative ratio of hydrogen in the samples. Comparing samples 2 and 3 where diluted silane is used, with 1 and 4 where undiluted silane is used, suggests lower hydrogen concentration for diluted samples (samples 2 and 3) with the least hydrogen concentration present in the sample 2 (i.e. the sample with the high He dilution).

It has been suggested that the device grade amorphous silicon film should contain between 8% and 12% atomic hydrogen [36]. Although various works have been done to determine the atomic percentage of hydrogen using FTIR, the values obtained using this method are not accurate and therefore not used in this work.

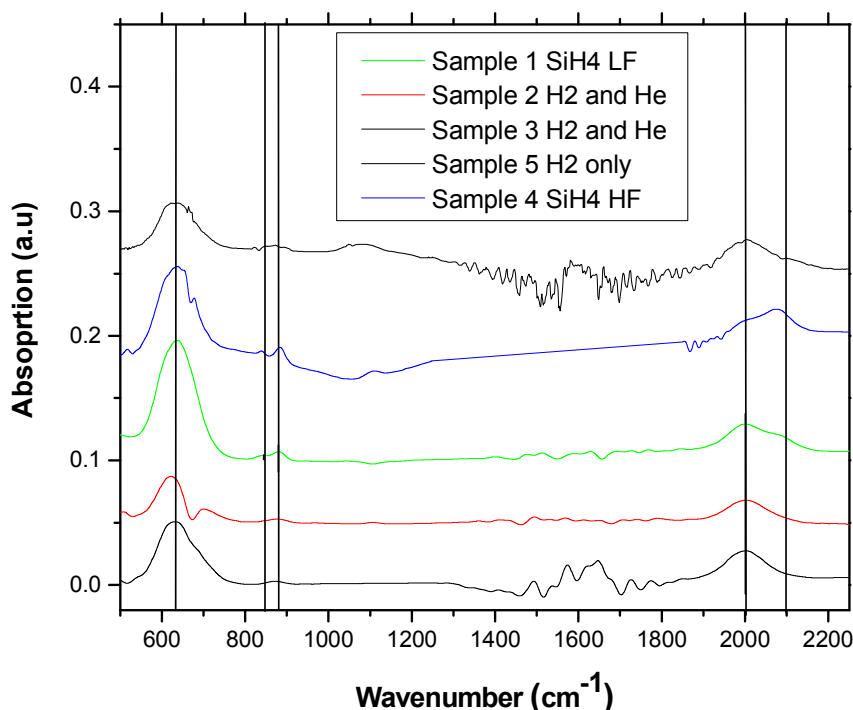


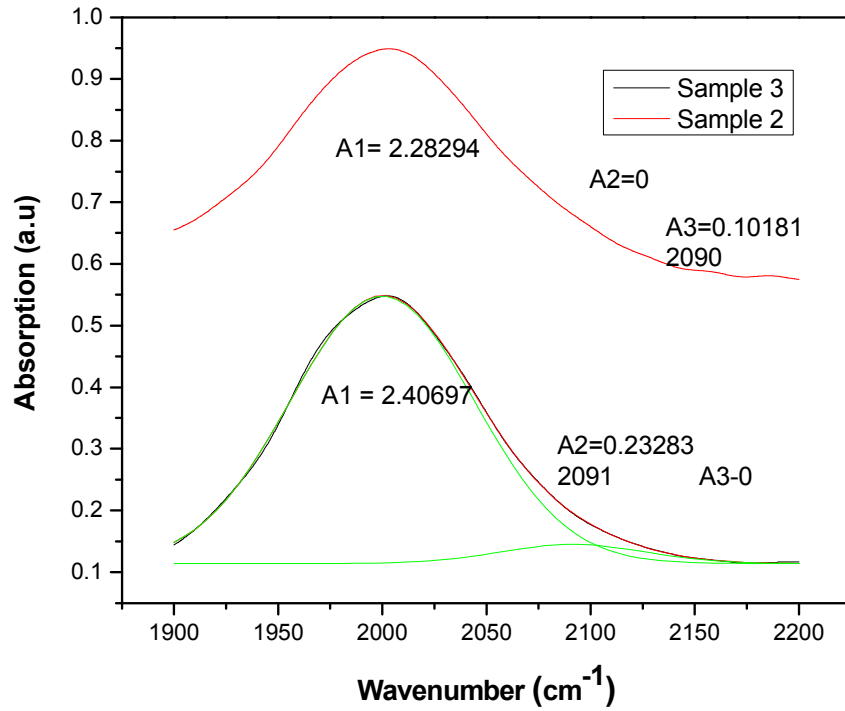
Figure 2-28 FTIR spectrum of low temperature a-Si:H samples

Schropp has defined the microstructure parameter  $R^*$  “as a figure of merit to indicate the hydrogen atoms that are not isolated Si-H bond surrounded by a dense network” of silicon.  $R^*$  is defined as [36]:

$$R^* = I_{2000}/(I_{2000}+I_{2060-2100})$$

$2000\text{cm}^{-1}$  is the Si-H stretching mode and the shift to higher wavenumbers of 2060 to  $2100\text{ cm}^{-1}$  is the result of Si-H in a less dense environment, e.g. voids, surface monohydrides, dihydride, clustered monohydride or dihydride. Schropp proposes an ideal  $R^* = 0$  and practical value of  $R^* < 0.1$  for a device grade a-Si:H film. However, this appears to be a ‘typing error’ as larger values of  $R^*$  are more suitable for device applications. Therefore  $R^* > 0.9$  is considered in this work.

In this work three Gaussians are fitted to the  $1900\text{ cm}^{-1}$  to  $2200\text{ cm}^{-1}$  range: one centred at  $2000\text{ cm}^{-1}$  and the remaining two between  $2060\text{ cm}^{-1}$  and  $2100\text{ cm}^{-1}$ . Figure 2-29 shows the deconvoluted peaks and area under each peak. The  $R^2$  values are better than 0.997 for both cases.  $R^*$  values obtained are 91% for sample 3 and 96% for sample 2, both within the expected range. Sample 5 has an  $R^*$  value of  $78 \pm 1.2\%$ , which is below the 90% requirement.

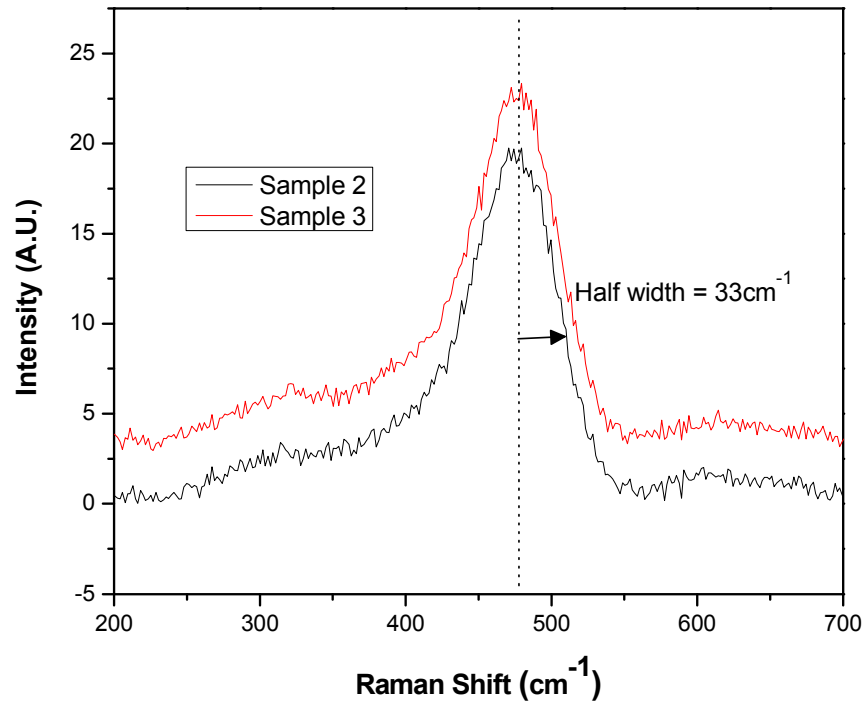


**Figure 2-29** FITR spectrum for samples 2 and 3 deconvoluted to three peaks at  $2000\text{ cm}^{-1}$  and the remaining two between  $2060\text{ cm}^{-1}$  and  $2100\text{ cm}^{-1}$ . A represents the area under the peaks.

The link between the short range order, the density of states [99], and the Urbach slope [100] has been observed for a-Si:H samples. The short range order can be extracted from Raman spectroscopy using the following empirical equation [101]:

$$L = 15 + 6 \cdot \Delta\phi$$

In here  $\Delta\phi$  is the RMS bonding angle deviation and L is the FWHM for the Raman peak. Figure 2-30 shows the Raman spectrum for samples 2 and 3. It can be seen that both samples have the same FWHM of  $66\text{ cm}^{-1}$ , corresponding to  $\Delta\phi = 8.5$ . This number is consistent with the expected value for low defect a-Si:H [99].



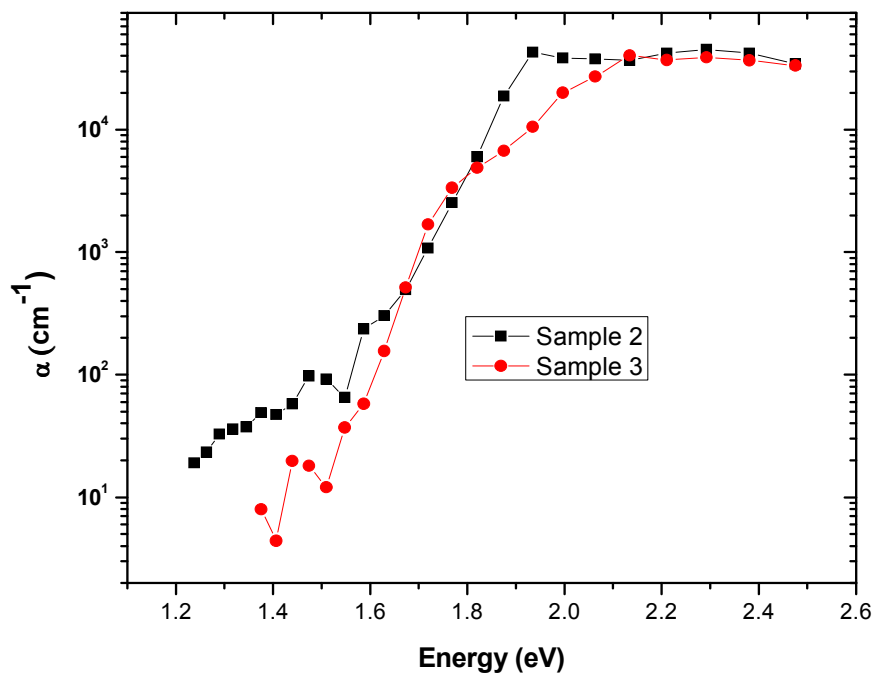
**Figure 2-30 Raman spectrum of amorphous silicon samples**

Figure 2-31 shows the absorption spectrum measured using CPM. The Urbach edge slope for sample 2 is 65 meV and for sample 3 is 45 meV. The requirement for device grade a-Si:H for solar cells is around 50mev [36] with sample 3 being within the expected range.

Absorption at higher wavelengths is indicative of the density of deep states. The absorption as measured with CPM does not provide the full information about the total density of states, although it has been used for the investigation of the density of states. Sample 3 has a lower absorption than sample 2, suggesting a lower density of states.

Sample 3 has a dark conductivity of  $5.7\text{E-}10$  S/cm and photoconductivity of  $5.5\text{E-}4$  S/cm and therefore a photoresponse of close to  $1\text{E}6$ . Although the dark conductivity is slightly high, the sample's electrical properties are within the requirements described in

Table 2-3. The slightly high dark conductivity could be due to the slightly n-type nature of intrinsic a-Si:H. Using the steady state photoconductivity measurement the mobility lifetime product of the sample is deduced as  $10\text{E-}7 \text{ cm}^2/\text{V}$  within the requirement for a-Si:H device grade material [36]. Sample 5 has a dark conductivity of  $3.4\text{E-}10 \text{ S/cm}$  and photoresponse  $1\text{E}5$ .



**Figure 2-31 Absorption spectrum of a-Si:H (i-layer) as measured using constant current measurement**

Optical properties of the i-layer play a critical role in the solar cell device properties. Optical and electrical properties of the amorphous silicon are interrelated, and optimised amorphous silicon must have certain optical characteristics. As discussed earlier, a Tauc bandgap of less than 1.8eV has been suggested for the intrinsic amorphous silicon layer. Figure 2-32 shows the Tauc plot of the amorphous silicon sample, sample 3. The sample had a bandgap of 1.75eV.



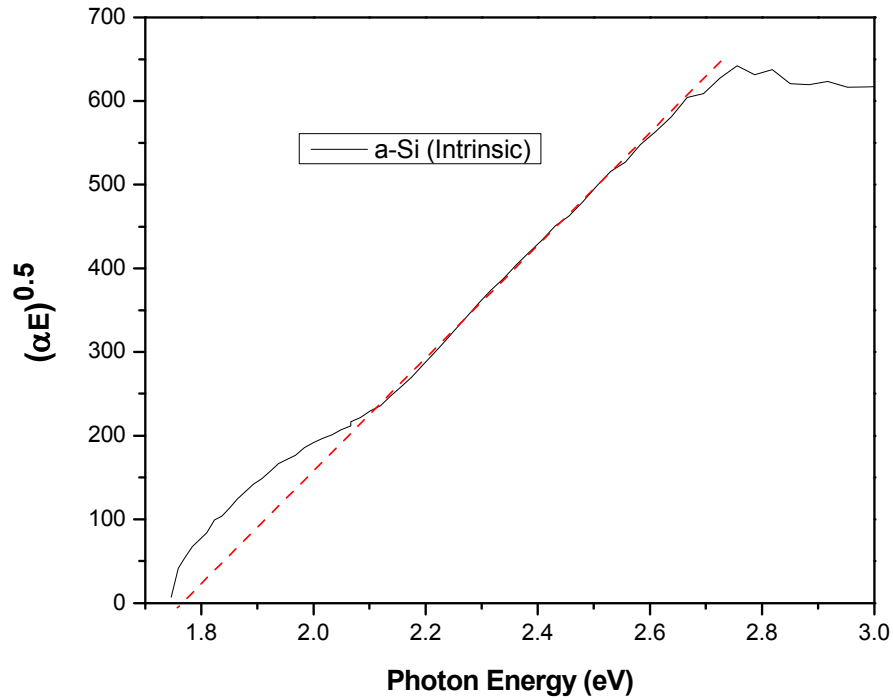


Figure 2-32 Tauc plot of intrinsic a-Si:H with bandgap of 1.75eV

### 2.6.2 Doped Layers

Boron doped a-SiC:H was used as the p-layer. The film was deposited using a process pressure of 0.6 Torr and plasma power of 5W using silane [8sccm]; 1% B<sub>2</sub>H<sub>6</sub> in H<sub>2</sub> [12sccm]; H<sub>2</sub> [12 sccm]; CH<sub>4</sub> [12sccm]. The film was deposited at 150°C. E04 is 2.2 eV and the bandgap from the tauc graph, Figure 2-33, is approximately 2eV. The sample has a resistivity of ~1E6 Ω cm.

A high flow rate of CH<sub>4</sub> was required to achieve the required bandgap. This could be due to the other deposition conditions (especially plasma power and pressure) used. Relativity high of doping concentration ([B<sub>2</sub>H<sub>6</sub>]/[SiH<sub>4</sub>]) of 1.5% was used in this work. For a p-i-n device a major issue with high boron doping is its diffusion into the i-layer [102]. For this reason a typically low B<sub>2</sub>H<sub>6</sub> doping concentration is used (e.g. 0.5%~1% [103][104][105][106]). However, given that the boron diffusion is a thermally activated

process [107], and that in this work p-i-n is deposited at a relatively low temperature, a higher  $[\text{B}_2\text{H}_6]/[\text{SiH}_4]$  was attempted.

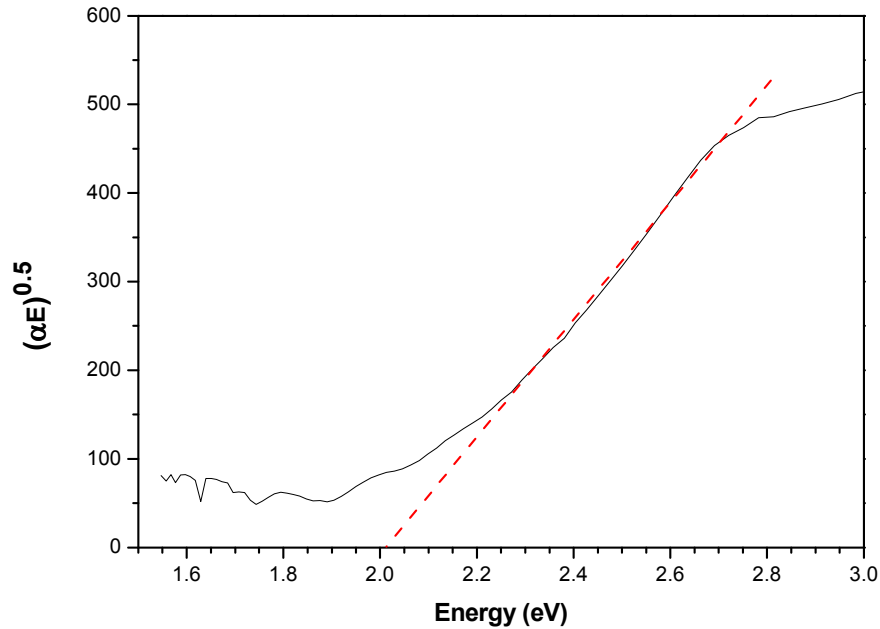


Figure 2-33 P-type a-SiC:H Tauc plot

## 2.7 Summary and Conclusions

In the first part of this chapter the main deposition tools and the common characterisation tools are described. The general approach for film deposition is investigated. The parameter extraction and measurement approaches are discussed.

An overview of different growth and transport mechanisms in nc-Si:H films was presented. Based on these, a range of nc-Si:H deposition conditions was selected. Growth rate, Raman shift, and dark conductivities were measured and discussed. A growth condition was identified, where the nc-Si:H exhibited characteristics consistent with a device quality film. Additional films needed for TFT fabrication (namely n-type

nc-Si:H contact layer and SiN:H gate dielectric) were deposited and qualified for the used in TFTs.

The growth of a-Si:H was studied. A number of films were deposited and their properties investigated. A suitable deposition condition for the growth of a-Si:H was identified. Different options for the window layer in the solar cell structure were considered and the a-SiC:H was identified as a suitable candidate. a-SiC:H as deposited for the window layer and its electrical and optical properties was characterised. The same n-type nc-Si:H used in TFTs was adopted as the n-layer for solar cells.

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## 3 Thin Film Transistor

### 3.1 Introduction

#### 3.1.1 Thin Film Transistor Operation

The thin film transistor is a field effect transistor operated in the accumulation/depletion modes [108]. For an n-type TFT, applying a positive gate voltage results in the filling of traps and accumulation of excess free electrons within the channel. As the gate voltage is further increased so does the density of free carriers, resulting in a more conductive channel. The rate of increase in channel conductance with increase in gate voltage is proportional to the field effect mobility,  $\mu_{FE}$ . The ratio of the transistor's conductivity in the “on” and “off” states is defined as the on/off ratio. It is desirable to have a transistor with high mobility and high on/off ratio.

Although many factors influence the conductivity of a channel, they can be grouped into three broad categories:

- Effective gate voltage: Electrostatic field in the channel. This is controlled by the gate voltage and flatband voltage. Flatband voltage is a function of gate dielectric and channel (e.g. trapped charge, mobile ions, and defect states).

- Channel material properties: Carrier mobility and type of transport in the channel influence its properties. For a disordered semiconductor, the density of tail states and the carrier mobility influence the channel conductivity [109].
- Channel Interface Properties: This is affected by carrier trap density at the interface of the channel- gate dielectric and at the channel- passivation interface. Also surface roughness at the interfaces is shown to influence carrier scattering and thus field effect mobility [110].

One further issue which would limit the *apparent* channel transconduction is the contact resistance which may include ohmic and non-ohmic components. This is discussed in the section 3.2. The *apparent* channel transconduction can also be enhanced by change in the charge distribution within the electric field. This is discussed in section 3.3.

## 3.2 Contact Resistance

Contact resistance has a significant impact on the electrical characteristics of thin film transistors (TFTs). It limits their maximum on-current and affects their subsequent behaviour with bias. This distorts the extracted device parameters, in particular the field-effect mobility. Contact resistance effects can reduce the voltage drop across the channel and limit the injected current. Contact effects are commonly minimised by using long-channel devices and/or highly-doped contacts. However, these strategies are not always possible, particularly at the research stage. For example the low process temperature, especially the absence of high temperature post-fabrication annealing, results in limited silicide formation at the metal-silicon interface or a defective doped silicon/silicon interface, leading to high and non-linear contact resistance.

In this section a method capable of accounting for both non-ohmic (non-linear) and ohmic (linear) contact resistance effects is developed. A 1-D device simulator (AMPS-1D) is used to investigate the presence of non-linear contact resistance and the validity of the technique. Finally, the effects of a number of different contact resistance mechanisms on the TFT field effect mobility are considered.

### 3.2.1 Non-linear Contact Resistance Extraction

The total resistance, composed of channel and contact resistances, is measured across the TFTs' output terminals. It is assumed that the channel resistance in the linear regime exhibits a purely ohmic behaviour. The contact resistance itself consists of ohmic and non-ohmic components. As shown below, the non-ohmic component can be mathematically described using a current-dependent polynomial, from which the total voltage drop across the device can be formulated:

$$V_{DS} = I_{DS} R_{Total} = R_{Channel} + R_{Contact}^{Ohmic} + R_{Contact}^{Non-Ohmic} = I_{DS} (R_{Channel} + R_{Contact}^{Ohmic} + (\sum_{i=2}^n A_i I_{DS}^{i-1})). \quad (3.1)$$

Here,  $V_{DS}$  represents the measured voltage drop;  $A_i$ s the constant coefficients of a polynomial;  $I_{DS}$  the drain-source current;  $R_{Contact}^{Ohmic}$  and  $R_{Contact}^{Non-Ohmic}$  the ohmic and non-ohmic components, respectively and  $R_{Channel}$  the channel resistance.

The ohmic component can be extracted using the well-established channel-length-scaling method for different gate voltages. Using the technique introduced in this section, the non-ohmic component can be isolated, allowing its value to be captured independently of the ohmic component. Knowing the complete contact resistance values and hence the actual voltage drop across the channel as a function of current, a method to obtain the true device parameters, including the field-effect mobility, is shown.

For a TFT biased in the linear regime, the drain-source current can be expressed as [111]:

$$I_{DS} = \frac{W}{L} \mu_{FE} C_i (V_{GS} - V_T) V_{Channel} \quad (3.2)$$

where  $V_{Channel}$  is the voltage across the channel;  $C_i$  the dielectric capacitance; and  $\mu_{FE}$  the field effect mobility. Differentiating equation (3.1) with respect to  $V_{GS}$  yields:

$$\left. \frac{\partial V_{DS}}{\partial V_{GS}} \right|_{V_{DS}} = \left[ I_{DS} \frac{\partial(R_{Total})}{\partial V_{GS}} \right]_{V_{DS}} + \left[ \frac{\partial I_{DS}}{\partial V_{GS}} \right]_{V_{DS}} (R_{Total}) \quad (3.3)$$

For each point of the transfer characteristics,  $(\partial V_{DS} / \partial V_{GS})|_{V_{DS}} = 0$  and  $(\partial I_{DS} / \partial V_{GS})|_{V_{DS}} = g_m^{measured}$  (*i.e.* transconductance). Thus:

$$g_m^{measured} = - \frac{V_{DS} \left[ \left. \frac{\partial R_{channel}}{\partial V_{GS}} \right|_{V_{DS}} + \frac{\partial(R_{Contact}^{Ohmic} + R_{Contact}^{Non-Ohmic})}{\partial V_{GS}} \right]_{V_{DS}}}{(R_{Channel} + R_{Contact}^{Ohmic} + R_{Contact}^{Non-Ohmic})^2} \quad (3.4)$$

The above equation can be solved to find the values of  $\mu_{FE}$  as a function of  $V_{GS}$ . Since  $\mu_{FE}$  is itself a function of  $V_{GS}$ , this equation can only be solved numerically for a given  $V_{DS}$ . The values of contact resistance as a function of  $V_{GS}$  will be retrieved from experimental data points.

The total resistance from the source to the drain terminals is the sum of channel, and ohmic and non-ohmic contact resistances. For a device operating in the linear regime:



$$R_{Total} = \frac{L}{W \mu_{FE} C_i (V_{GS} - V_T) V_{Channel}} + R_{Contact}^{Ohmic} + R_{Contact}^{Non-Ohmic} \quad (3.5)$$

where  $R_{Total}$  can be obtained from terminal current-voltage characteristics.

The following technique can be used to capture the non-linear component of contact resistance. The total voltage drop across the device,  $V_{DS}$ , can be written as:

$$V_{DS}(I_{DS}) = V_{Channel}(I_{DS}) + V_{Contact}^{Ohmic}(I_{DS}) + V_{Contact}^{Non-Ohmic}(I_{DS}).$$

Here,  $V_{Contact}^{Ohmic}$  represents the first order term and  $V_{Contact}^{Non-Ohmic}$  the higher order terms. The operator  $[\partial F(x)/\partial x - F(x)/x]$  can remove the first order terms in a series expansion of function,  $F(x)$ . Applying this to  $V_{DS}(I_{DS})$ :

$$\left. \frac{\partial V_{DS}}{\partial I_{DS}} \right|_{V_{GS}} - \frac{V_{DS}}{I_{DS}} = \left. \frac{\partial V_{Contact}^{Non-Ohmic}}{\partial I_{DS}} \right|_{V_{GS}} - \frac{V_{Contact}^{Non-Ohmic}}{I_{DS}} = \sum_{i=2}^n a_i I_{DS}^{i-1} = R_{Contact}^{Non-ohmic} \quad (3.6)$$

where  $a_i = (i-1)A_i$ . Note that  $R_{Channel}$  and  $R_{Contact}^{Ohmic}$  are both ohmic, therefore:

$$\left( \frac{\partial V_{Channel}}{\partial I_{DS}} \right) \Big|_{V_{GS}} - V_{Channel}/I_{DS} = 0 \text{ and } \left( \frac{\partial V_{Contact}^{Ohmic}}{\partial I_{DS}} \right) \Big|_{V_{GS}} - V_{Contact}^{Ohmic}/I_{DS} = 0.$$

Using the channel-length-scaling method,  $R_{Contact}^{Ohmic}$  can be extracted for different  $V_{GS}$  values. We then retrieve  $R_{contact}^{Non-Ohmic}$  as a function of  $I_{DS}$  at different  $V_{GS}$  points. The sum of the ohmic and non-ohmic components yields the total value of contact resistance.

### 3.2.2 Validity of Non-linear Contact Resistance Method

Having developed a strategy to quantify both linear and the non-linear components of contact resistance, it is important to check the validity of this approach when

extracting the non-linear contact resistance. A one-dimensional device simulator is used for this purpose.

A TFT is a 2-D device and a 1-D device simulator would never fully describe its properties. However, as described here, an attempt is made to probe contact properties for a limited case. As shown in Figure 3-1, the TFT channel can be considered as a number of “thin” parallel channels. The “thin” channel closest to the gate dielectric experiences the highest electric field and therefore has the highest density of accumulated charge. The density of these carriers can be estimated along the channel depth by performing a 1-D simulation of a MIS structure. This is shown in Figure 3-2, where the channel is a-Si:H and the gate is 300nm silicon nitride. Appendix 1 outlines the material properties used in this work.

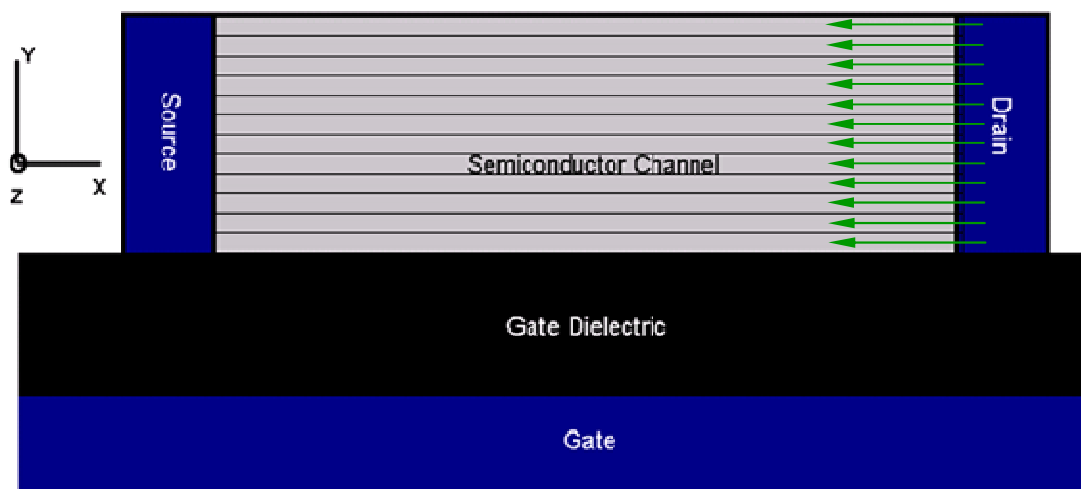


Figure 3-1 TFT cross section

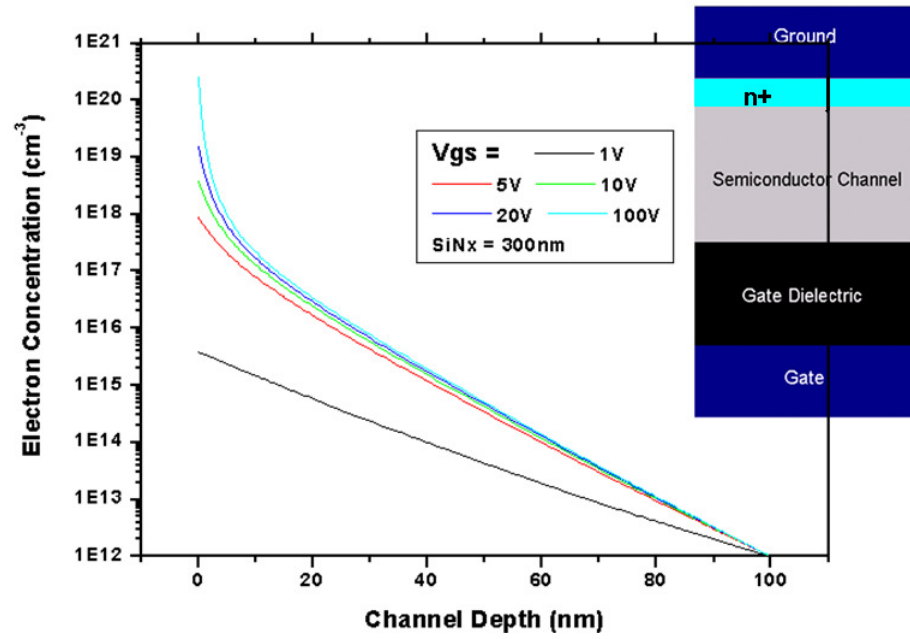


Figure 3-2 Electron carrier concentration as a function of channel depth for different gate voltages

Values of free carriers in the MIS structure can be used in the simulation of a 1-D metal/a-Si:H/metal structure to investigate contact effects. Figure 3-3 shows the cross sectional diagram for the simulated structure. This approach is based on the assumption that  $V_{gs} > V_{ds}$  and thus carrier concentration in the lateral direction is essentially constant. No doped contact layer was used. A metal/semiconductor barrier height of 0.5eV was used in this work. A large-barrier without doping was used as an extreme case.

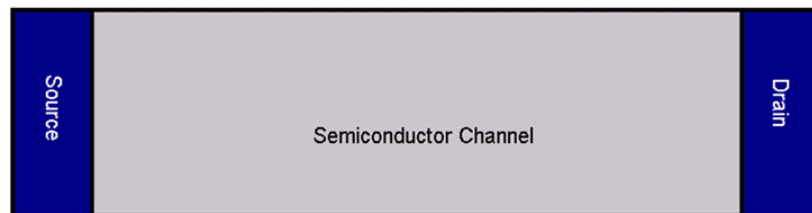
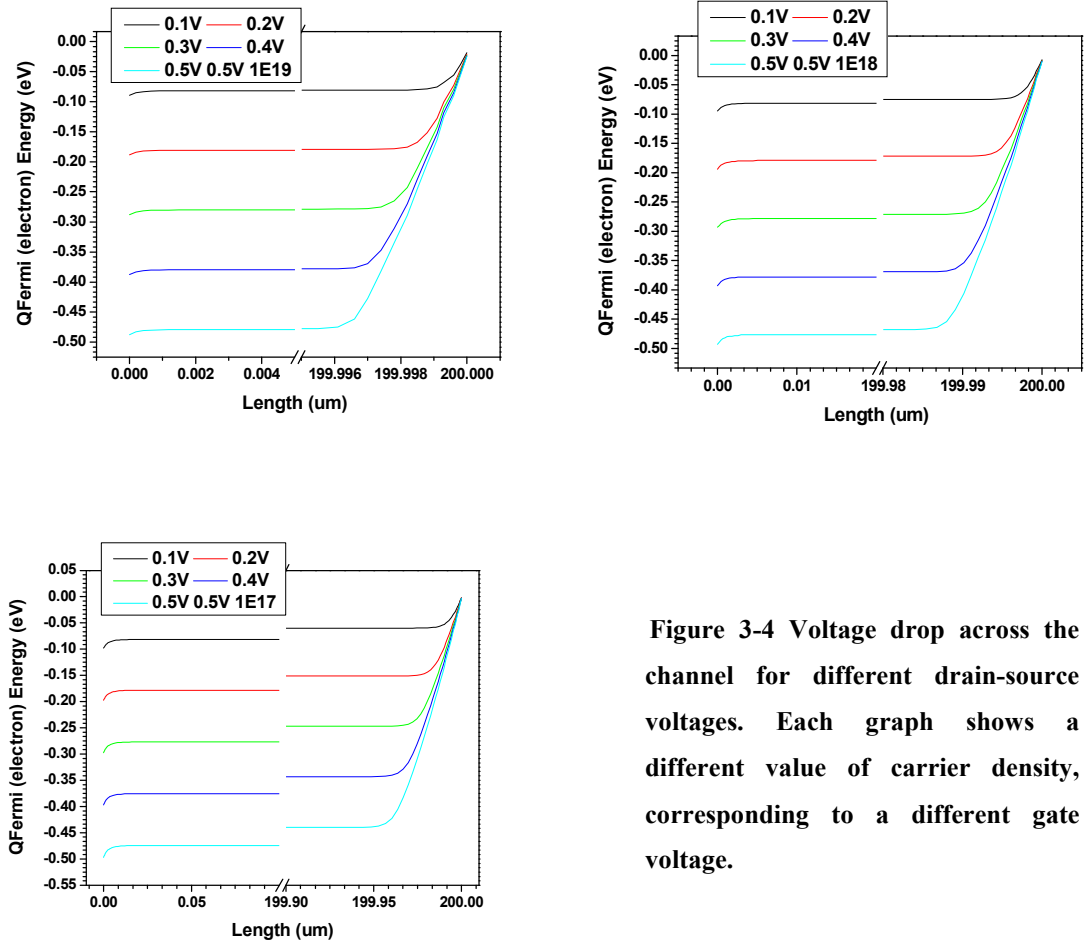


Figure 3-3 Cross sectional diagram of 1-D metal/a-Si:H/metal simulation

The results of the simulation are shown in Figure 3-4. The electron quasi-fermi level represents the voltage drop relative to the source. A large  $V_{ds}$  dependent voltage drop

can be seen on the source side of the device. This is a voltage drop across the reverse biased schottky barrier at the source. An additional, smaller, voltage drop across the forward biased schottky barrier (drain) can be seen.



**Figure 3-4 Voltage drop across the channel for different drain-source voltages. Each graph shows a different value of carrier density, corresponding to a different gate voltage.**

In addition to the 200um channel length, the simulation is repeated for 50, 100 and 150um. By applying the extraction method outlined in 3.2.1 the linear and non-linear contact resistance is extracted from the current voltage characteristics. Figure 3-5 compares the contact resistance extracted from I-V curves with the one extracted from the shift in the electron quasi-fermi level. It can be seen that applying the scaling method alone results in a significant underestimate of the contact resistance, especially at higher voltages. However, combining the non-linear and linear methods can result in

an improved estimate of the contact resistance. It should be noted that an excellent linear fit was made when extracting linear contact resistance using the scaling method.

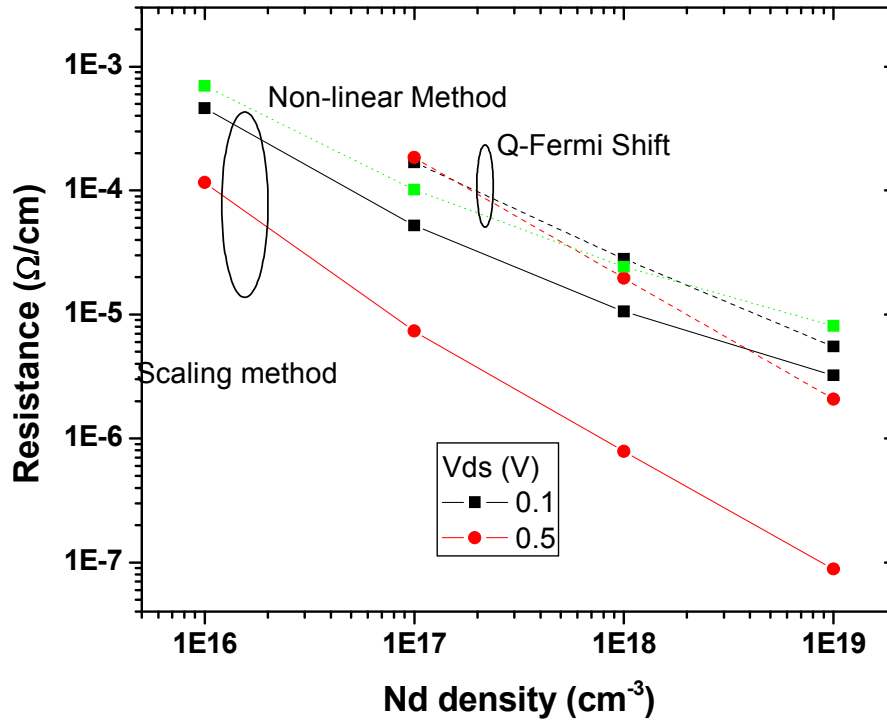


Figure 3-5 Contact resistance vs. Carrier density for different  $V_{ds}$  values

### 3.2.3 Effect of Contact Resistance on Field Effect Mobility

Contact resistance has been attributed to a number of mechanisms such as current crowding [112], constant parasitic resistance, transport through barrier [113], and defects at the contact interface [114]. Depending on the materials used, and the device structure and operating voltages, some of the mechanisms are more applicable than others. Contact resistance can significantly change the TFTs' transconductance, effecting both its dependence on the gate voltage and the peak value. This section briefly looks at the effect of a few types of contact resistance on the transconductance characteristics.

The relation between band mobility and the field effect mobility of a device with a disordered semiconductor channel follows the equation below [115]:

$$\mu_{eff} = \frac{n_{free}}{n_{trapped} + n_{free}} \mu_{band} \quad (3.7)$$

$n_{trapped}$  and  $n_{free}$  are the sheet density of trapped and free carriers across the channel (per  $\text{cm}^{-2}$ ).

To simulate  $n_{trapped}$  and  $n_{free}$ , AMPS-1D was used to calculate the density of free and trapped carriers at different locations across the depth of the channel for different gate voltages in an MIS structure. The approach used is shown in Figure 3-2 which also shows the free carrier densities used for this part.

These values were integrated across the depth of channel to give the sheet charge density for both trapped and free carriers. It was confirmed that the total sheet density (free and trapped carriers) are consistent with the density of induced charge from the electric field calculation. A wide range of band mobility for a-Si:H has been reported [116] although a value of  $10\text{cm}^2/\text{V.s}$  has been used for some of the calculations [117].

To make the comparisons clearer  $\frac{\mu_{FE}}{\mu_{band}}$  is used.

Figure 3-6 and Figure 3-7 show the effect of the deep and shallow state density on the field effect mobility. It can be seen that the change in the gap state defect density results in the shift of  $\frac{\mu_{FE}}{\mu_{band}}$  (effectively a change in the  $V_t$ ), whereas change in the shallow state density results in the degradation of the field effect mobility. This is consistent with the simulation result from [109].

These results can qualitatively be explained as follows: in order to switch on a TFT the Fermi-level needs to move to the edge of the band-tail states. This is achieved by applying a voltage, to accumulate enough charge, and to fill the deep state traps (localised states). An increase in the defect state density results in a need for a higher charge accumulation density leading to a higher turn on voltage. On the other hand, an increase in the extended state results in a decrease in  $\mu_{FE}/\mu_{band}$  as described by equation(3.7).

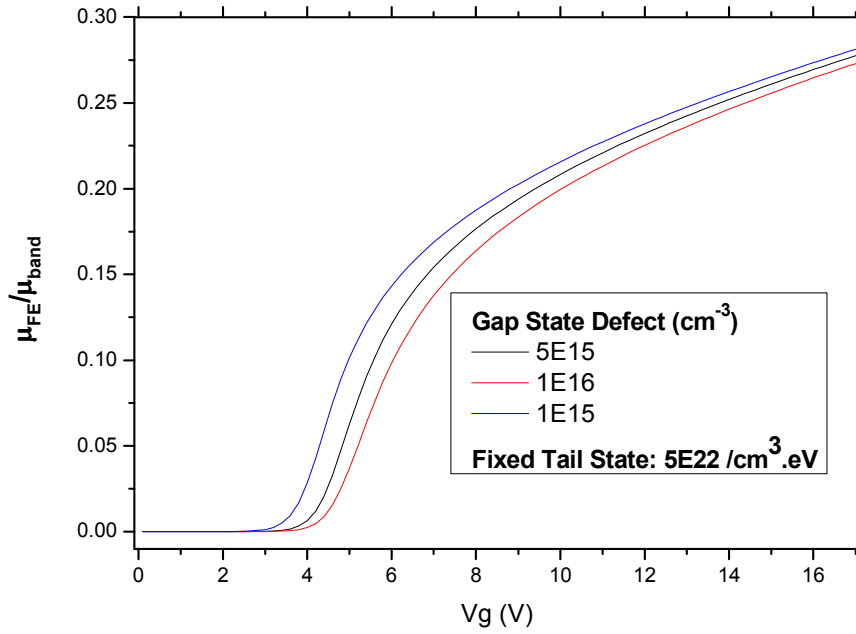


Figure 3-6 Effect of gap state defect density on  $\mu_{FE}/\mu_{band}$

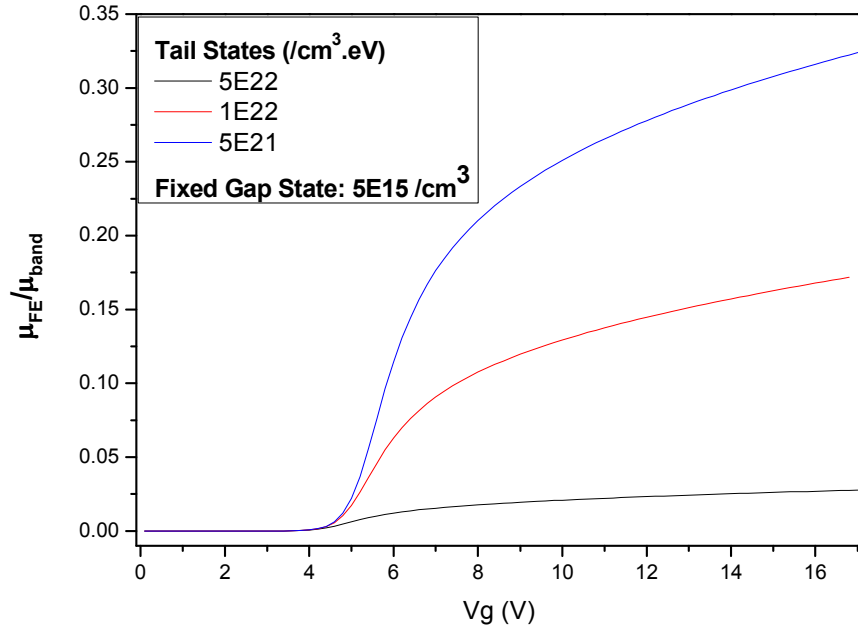


Figure 3-7 Effect of tail state defect density on  $\mu_{FE}/\mu_{band}$

Having considered the effect of the channel defect density on the shape of  $\frac{\mu_{FE}}{\mu_{band}}$  it

is possible to consider the effect of the contact resistance on the  $\frac{\mu_{FE}}{\mu_{band}}$  curve by solving

equation (3.4). In this equation  $R_{channel}$  is the channel resistance and can be written as

$$R_{channel} \propto (\mu_{band} \sigma_{free} q)^{-1} [115]. \text{ When considering contact resistance the ratio of } \frac{R_{channel}}{R_{contact}} \text{ is}$$

important and this is considered in the rest of this work.

The simplest case of contact resistance is the one which is independent of gate voltage. Figure 3-8 shows the effect of different values of constant contact resistance on mobility. A peak-and-drop feature can be observed, although for the smallest value of

constant resistance (i.e.  $\frac{R_{channel}}{R_{contact}} = 10$ ) no peak can be seen on the graph.



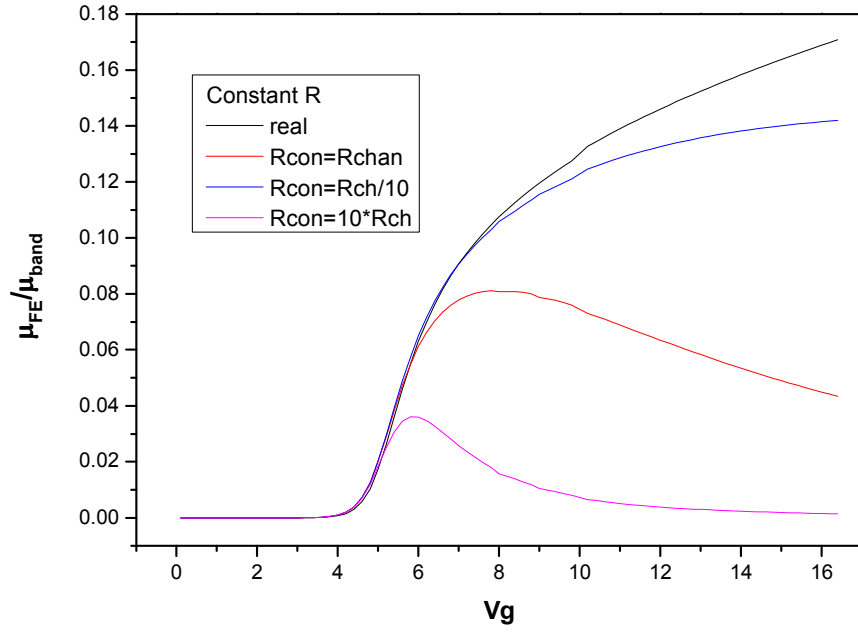


Figure 3-8 Effect of constant contact resistance on  $\frac{\mu_{FE}}{\mu_{band}}$

The behaviour for this can be explored by examining the equations below which relates  $g_m^{measur}$  to  $g_m^{real}$ . Two special cases of constant contact resistances are shown below. The first one shows a large CR and the second a small contact resistance.

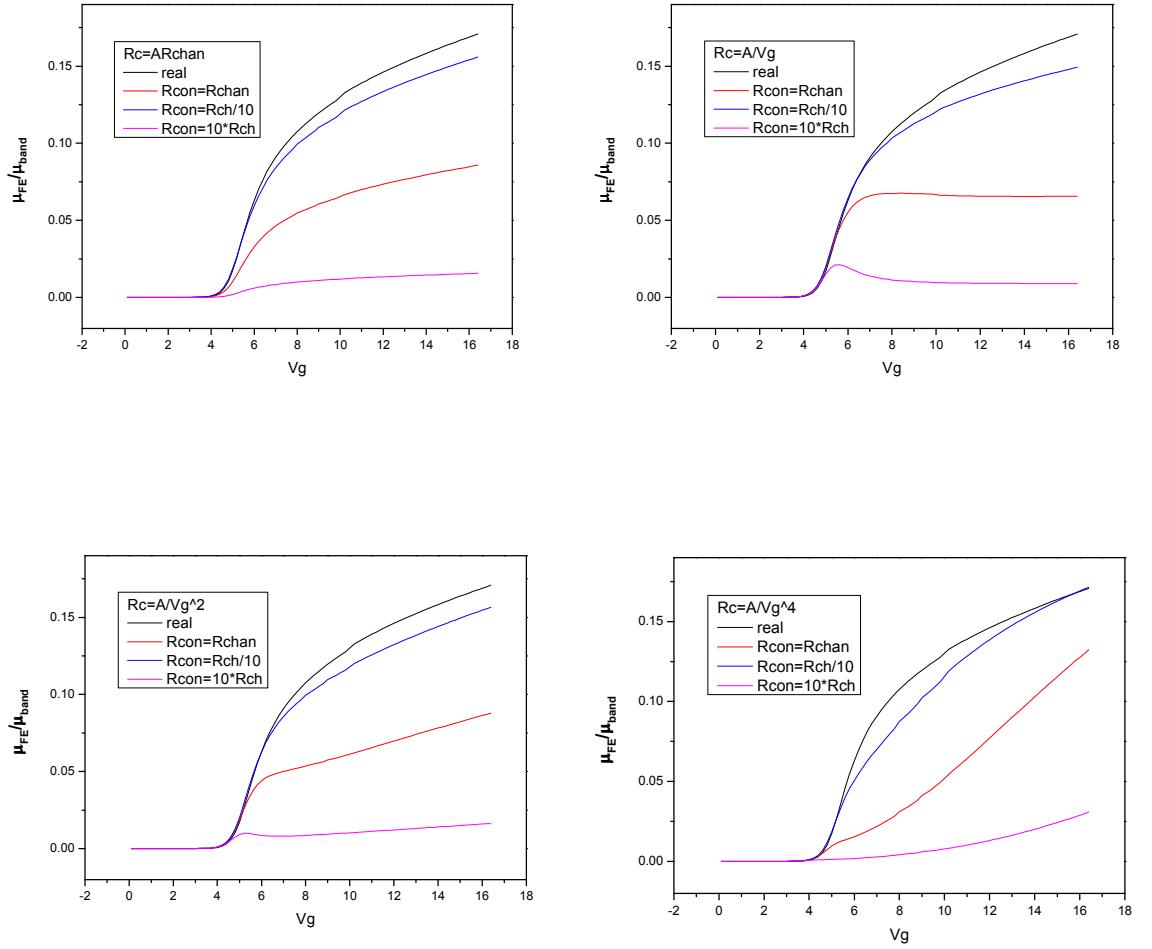
$$g_m^{measured} = \frac{g_m^{real} \cdot V_{DS}^2}{(V_{DS} + g_m^{real} \cdot R_{contact} \cdot V_{GS})^2} \quad (3.8)$$

$$V_{DS} \ll g_m^{real} \cdot R_{contact} \cdot V_{GS} \Rightarrow g_m^{measured} = \frac{V_{DS}^2}{R_{contact}^2 \cdot V_{GS}^2} \times \frac{1}{g_m^{real}} \quad (3.9)$$

$$V_{DS} \gg g_m^{real} \cdot R_{contact} \cdot V_{GS} \Rightarrow g_m^{measured} = \frac{g_m^{real} \cdot V_{DS}^2}{(V_{DS})^2} = g_m^{real} \quad (3.10)$$

It can be seen that the peak is the result of the superposition of two cases. For smaller values of the gate voltage (where  $V_{DS} \gg g_m^{real} \cdot R_{contact} \cdot V_{GS}$ ) the curve follows the true field effect mobility. However, as the gate voltage increases such that  $V_{DS} \ll g_m^{real} \cdot R_{contact} \cdot V_{GS}$ , the mobility becomes inversely proportional to the square of the gate voltage and the true field effect mobility. Therefore for  $\frac{R_{channel}}{R_{contact}} = 10$  in the previous example, the peak and drop are expected to occur at a larger gate voltage.

For the case of current crowding a number of relations between  $R_{channel}$  and  $R_{contact}$  have been proposed. They include  $R_{contact} \propto R_{channel}$  and  $R_{contact} \propto V_{gs}^{-n}$  where n in the range of 1 to 4 has been reported [118][119]. Figure 3-9 shows the effect of different current crowding models on the  $\frac{\mu_{FE}}{\mu_{band}}$ . It can be seen that unlike the constant resistance test case which results in a continuous drop, current crowding results in either a continuous rise or flattening (when  $R_{contact} \propto V_{gs}^{-1}$ ).

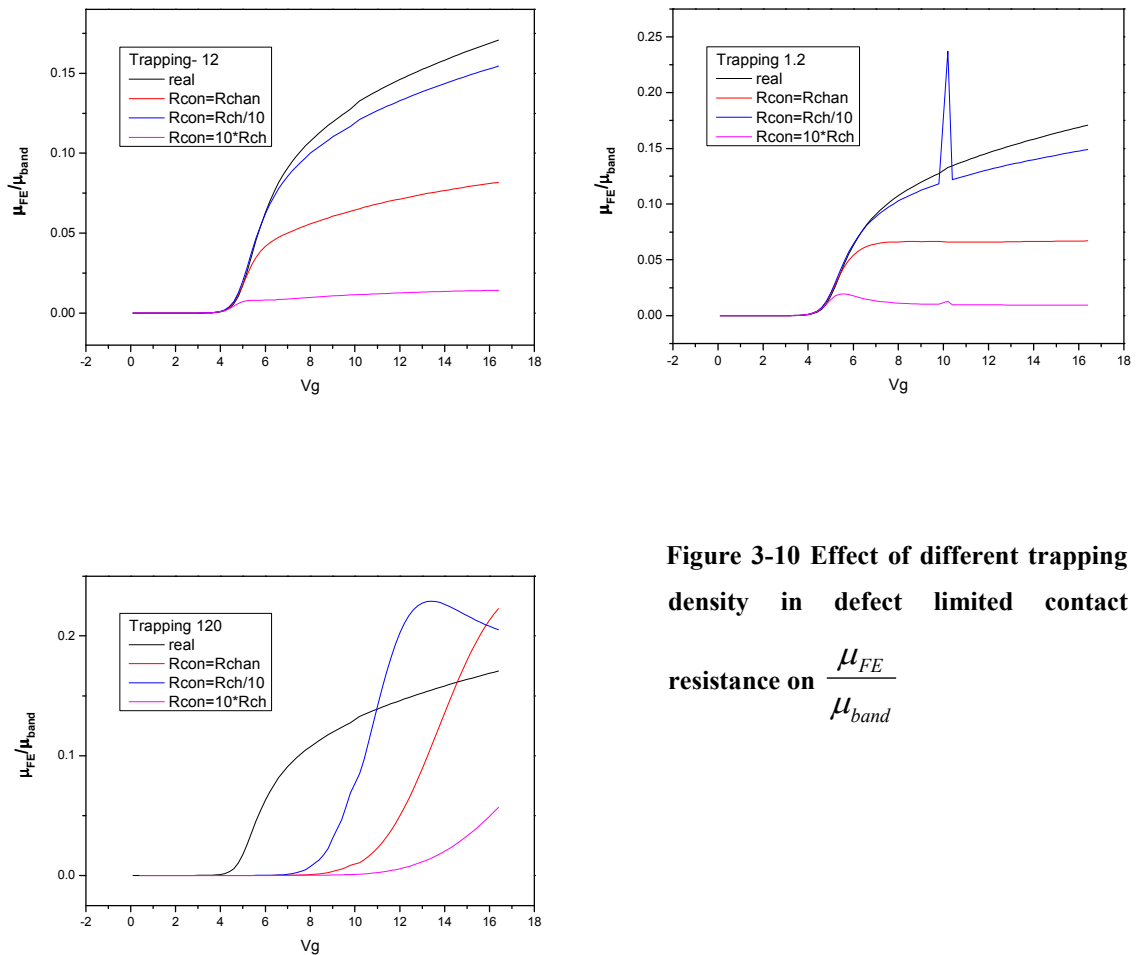


**Figure 3-9** Effect of different current crowding models on the  $\frac{\mu_{FE}}{\mu_{band}}$

Contact resistance can also be due to transport over a barrier with electronic defect states. As a gate voltage is applied the defects are filled and the barrier height changes. In this work the grain boundary transport model, in line with the works of Vinciguerra et al., was used [114]. Equation (3.11) was used in this calculation.

$$R_c = R_{c0} \cdot \exp \left[ \frac{q^3 N_t^2 t}{8 \epsilon C_i k T} \frac{1}{V_G - V_{th}} \right] \quad (3.11)$$

Figure 3-10 shows the effect of different values of trap density on field effect mobility behaviour. Each of the graphs shows different contact trapping densities used in this work. The values of the remaining parameters are set to achieve the desired  $R_{con}/R_{chan}$ . These results suggest that for low trap density the mobility saturates. However, as the trapping density is increased, due to the combined effect of charge accumulation in the channel and drop in the contact resistance, mobility increases significantly, although this is followed by a short drop in the mobility.



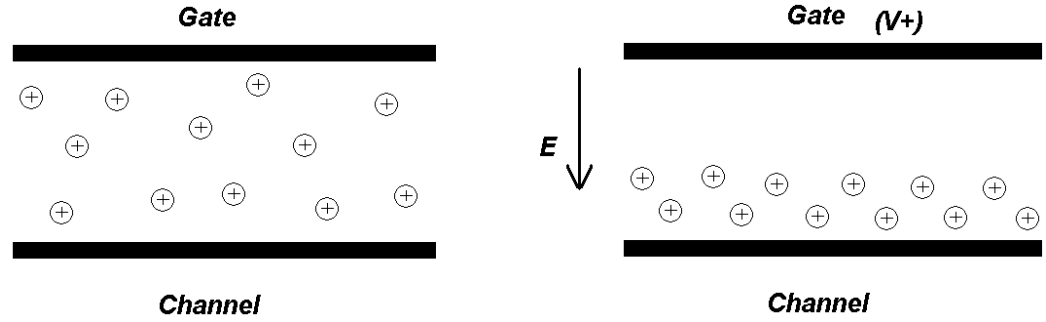
**Figure 3-10 Effect of different trapping density in defect limited contact**

resistance on  $\frac{\mu_{FE}}{\mu_{band}}$

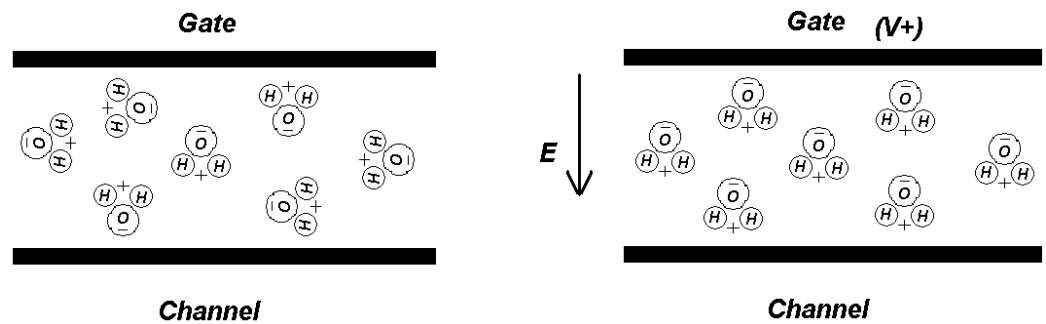
### 3.3 Dynamic Threshold Voltage Shift

M. J. Powell used the phrase “dynamic threshold voltage shift” to describe the shift in flatband voltage as a result of charge redistribution between the tail states and the deep states in a-Si:H channel of a thin film transistor [108]. This process takes place after an accumulation of excess carriers and may take a few 100ms. It results in a reduction of drain-source current as the TFT is switched on. A *dynamic threshold voltage shift* process in the negative direction results in the increase of  $V_g - V_t$  with time, and therefore an increase in drain-source current with time.

One possible source of such a dynamic threshold shift is the drift of mobile charges in the gate dielectric as the result of the transverse electric field induced by the voltage across the dielectric. Regardless of the polarity of the mobile charge, the direction of ionic drift is such that this process would result in an increase in the  $V_g - V_t$ . Figure 3-11 highlights the process for an n-channel device as it is switched on. Such an effect was observed in the early days of the c-Si field effect transistors [120]. However, historically, the  $V_T$  shift rate at room temperature has been too slow for any practical application and thus steps were taken to minimise it. A similar effect may take place as the result of dipole polarisation [121] as shown in Figure 3-12. However it has been shown in recent works that the time scale for such a shift is fast in PECVD oxide gate dielectrics, particularly the ones deposited at lower temperatures [122][123]. This describes the possible enhancement in such devices as a result of mobile ion drift. Although the time scale of the  $V_t$  shift is too slow for the devices to be used as switches, they may still be useful as *power TFTs* (analogy to power FETs).



**Figure 3-11** Mobile ions drift inside the dielectric resulting in the enhancement of the channel field



**Figure 3-12** Polarisation of dipoles inside the gate dielectric under electric bias is applied across the gate dielectric.

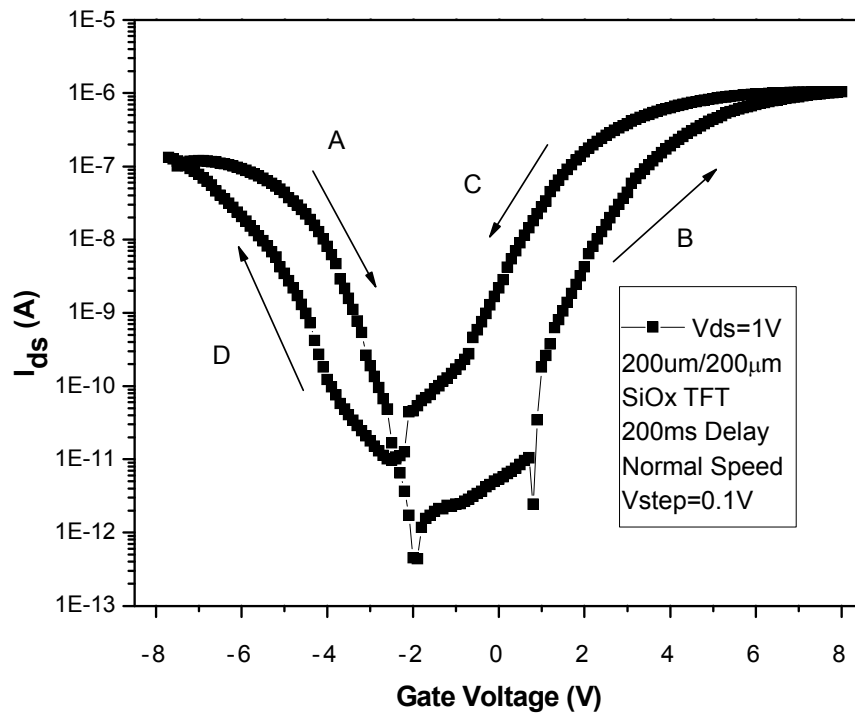
No TFT device has been fabricated for this report. The following section describes the results of measurements performed on devices which exhibit the properties intended to be used in this work. The devices used here are top gate nc-Si:H TFTs with low temperature silicon oxide gate dielectric. Full deposition conditions are reported elsewhere [26].

### 3.3.1 Sweep Gate Measurement

When the measurement time is comparable with the dynamic threshold voltage shift of a device, hysteresis is observed in the transfer characteristics of that device. The hysteresis may be clockwise when  $V_G - V_T$  reduces with time (e.g. deep-trap filling process) or anticlockwise when  $V_G - V_T$  increases with time (e.g. ionic drift, dipolar polarisation).

Figure 3-13 shows the anticlockwise direction of the hysteresis for a device with low temperature silicon oxide, demonstrating the fact the  $V_G - V_T$  increases with time. It should be noted that the hysteresis is a function of measurement time setting and therefore the curve in

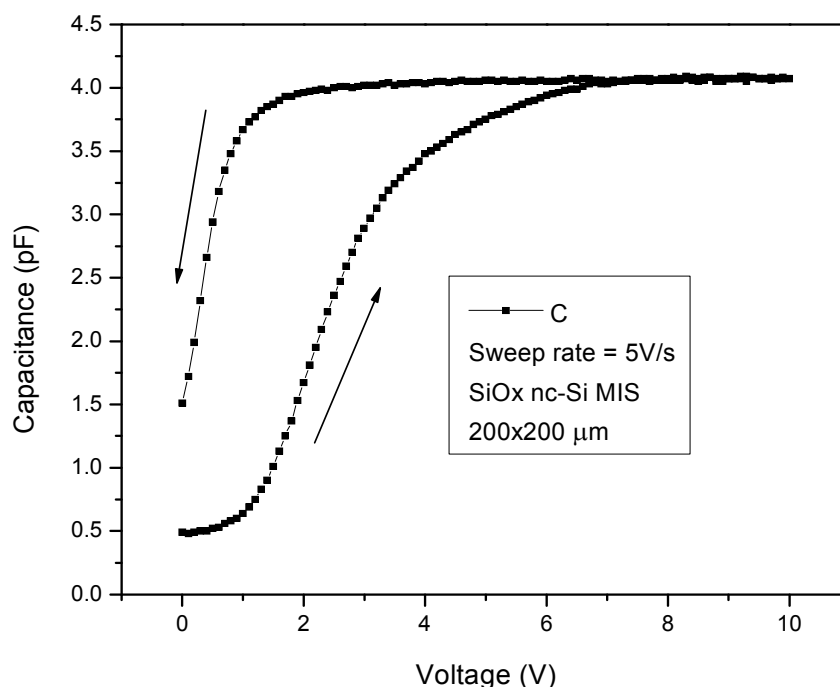
**Figure 3-13** would change significantly depending on the speed and voltage steps used in the measurement.



**Figure 3-13 Hysteresis in the transfer characteristics of a device with low temperature silicon oxide**

To confirm that the hysteresis is due to the dielectric, capacitance-voltage measurement was performed on a MIS structure on the same substrate. The application of a positive gate voltage, results in a negative shift of  $V_T$  and increase in  $V_G - V_T$  as shown in

Figure 3-14. Any possible movement of ions (or dipolar polarisation) would result in a gate current which can be detected externally. Applying a slow triangular voltage ramp across the gate-channel whilst monitoring the gate current allows detection of ionic drift (or dipole polarisation) [124]. This measurement is normally performed at elevated temperatures to enhance the movement of mobile ions and allow their detection.



**Figure 3-14 Capacitance voltage measurement on a MIS structure with low temperature silicon oxide dielectric.**

Figure 3-15 shows the gate leakage current as a function of gate voltage at room temperature when a triangular voltage ramp of between -3V to 3 V with a frequency of 10mhz is applied to the gate. Low frequency is used to minimise the capacitor charging current. The presence of a loop in Figure 3-15 demonstrates the mobile-ion drift (or dipolar polarisation). Similar results have been obtained for devices with dipoles in the



dielectrics and therefore this measurement does not rule out either mechanism [124]. The area inside the loop corresponds to two times the total mobile-ion charge (or effective dipolar charge). This measurement was performed at room temperature and the observation of such a loop at room temperature suggests that the dynamic  $V_T$  shift is a relatively fast process at room temperature.

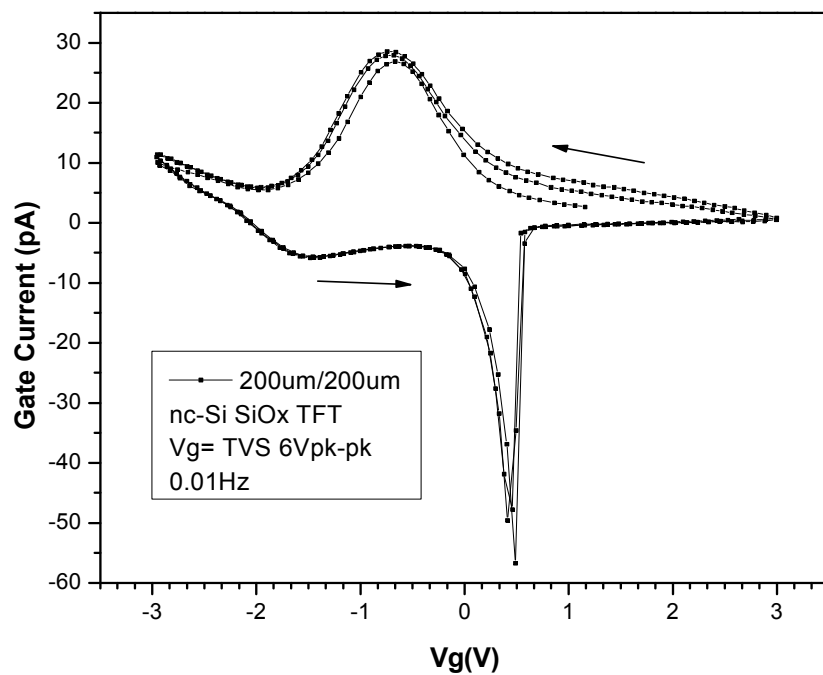


Figure 3-15 Gate current under application of a triangular voltage ramp at room temperature

### 3.3.2 Static Measurement

The field effect (FE) mobility of thin film transistors (TFTs) is normally extracted using static measurement methods, which inherently rely on the assumption that the device remains stable during the measurement duration. However, these devices, particularly those based on newly emerging materials, can show large instability during the measurement, typically exhibiting hysteresis in the static characteristics. This section looks at the effect of threshold voltage shift on field effect mobility extracted

using the conventional method, and introduces an alternative, and more accurate, technique of measuring device characteristics. The technique decouples the effect of transient phenomena and thus permits extraction of the true device field effect mobility, which turns out to be either over or underestimated depending on the magnitude and direction of the threshold voltage shift.

The effective FE mobility,  $\mu_{FE}$ , in a TFT is an important geometry independent parameter widely used in device modelling. The  $\mu_{FE}$  is commonly extracted from the channel transconductance (i.e. first order derivative of the transfer characteristics). However, if the transfer characteristics are distorted by external effects, the value of  $\mu_{FE}$  extracted no longer represents a true channel property. Two effects can influence the transfer characteristics: the source/drain contact resistance and the instability of the TFT during measurement. In section 3.2 it was demonstrated that the contact resistance, both linear and non-linear components, can result in an underestimation of  $\mu_{FE}$ . To deal with the latter, we introduce an alternative extraction technique based on a constant current measurements. This technique, highly suited for unstable devices, provides a means to decouple the effect of threshold voltage shift ( $\Delta V_T$ ) on the extraction of  $\mu_{FE}$ .

Depending on the measurement time settings, the transfer characteristics can take several minutes to complete. Generally it is assumed that the TFTs are stable enough to have a negligible  $\Delta V_T$  during this time and therefore the standard measurement method based on gate voltage sweeping can be used. Consider the behaviour of a device operating in the linear range (i.e.  $V_{GS} - V_T \gg V_{DS}$ ),

$$I_{DS} = \mu_{FE} \frac{W}{L} C_i (V_{GS} - V_T) V_{DS} \quad (3.12)$$

where  $W$  and  $L$  are channel width and length and  $C_i$  is the gate dielectric capacitance. The equation above can be differentiated with respect to the gate voltage to yield the transconductance; i.e:

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} \frac{W}{L} C_i \left[ \frac{\partial V_{GS}}{\partial V_{GS}} - \frac{\partial V_T}{\partial V_{GS}} \right] V_{DS} \quad (3.13)$$

If we assume that  $\frac{\partial V_{GS}}{\partial V_{GS}} = 1$  and  $\frac{\partial V_T}{\partial V_{GS}} = 0$ , we arrive at the standard definition of the

transconductance, widely used to extract the effective FE mobility:

$$g_m = \mu_{FE} \frac{W}{L} C_i V_{DS} \quad (3.14)$$

The assumption  $\frac{\partial V_T}{\partial V_{GS}} = 0$  is only true if  $\partial V_T \ll \partial V_{GS}$ . Therefore, in an unstable device  $\frac{\partial V_T}{\partial V_{GS}} \neq 0$ . Expanding Eqn. (3.12) to include the fixed ( $V_{T0}$ ) and time-dependent (

$V_T(t)$ ) components of the threshold voltage yields

$$I_{DS} = \mu_{FE} \frac{W}{L} C_i [V_{GS} - V_{T0} - V_T(t)] \cdot V_{DS} \quad (3.15)$$

Differentiating Eqn. (3.15) with respect to the gate voltage:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} \frac{W}{L} C_i \left[ \frac{\partial V_{GS}}{\partial V_{GS}} - \frac{\partial V_{T0}}{\partial V_{GS}} - \frac{\partial V_T(t)}{\partial V_{GS}} \right] \cdot V_{DS} \quad (3.16)$$

in which  $\frac{\partial V_{GS}}{\partial V_{GS}} = 1$  and  $\frac{\partial V_{T0}}{\partial V_{GS}} = 0$ . We now have an additional term:

$$\frac{\partial V_T(t)}{\partial V_{GS}} = \frac{\partial V_T(t)/\partial t}{\partial V_{GS}/\partial t} \neq 0 \text{ that remains. Thus}$$

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} \frac{W}{L} C_i \left[ 1 - \frac{\partial V_T(t)}{\partial V_{GS}} \right] \cdot V_{DS} \quad (3.17)$$

Depending on the direction of  $\Delta V_T$ , (i.e. the sign of  $\partial V_T(t)/\partial t$ ) this additional term can be positive or negative, resulting in an over or underestimation of the true  $\mu_{FE}$ .

Clearly the type of  $\Delta V_T$ , which affects the static characteristics of a TFT are too fast to be observed using standard static measurement methods. The approach taken in this work is to use a closed feedback control loop to adjust the gate voltage to maintain a constant drain-source current for a fixed drain-source voltage. Assuming a constant current and a constant drain-source voltage,  $V_{GS}(t) - V_{T0} - V_T(t)$  in eqn. (4) is a constant to yield:

$$\frac{\partial V_T(t)}{\partial t} = \frac{\partial V_{GS}(t)}{\partial t} \quad (3.18)$$

whereby the shift in threshold voltage is equal to the shift in gate voltage. The measurement set-up is implemented in software using the Keithley 4200-SCS semiconductor characterisation system, in which the control loop utilises a discrete proportional, integral, derivative (PID) algorithm. A 25-sec time window was used for monitoring the effect of  $V_T$  shift on the transfer characteristics, and was found to be sufficient in terms of observing any abnormalities.

The above set-up was used to measure the  $\Delta V_T$  of nanocrystalline silicon (nc-Si:H) TFTs with two types of gate dielectric: silicon nitride (SiN:H<sub>x</sub>) and silicon oxide (SiO<sub>x</sub>). Both devices were deposited on Corning 1737 glass substrate using RF plasma enhanced chemical vapour deposition (PECVD). The deposition conditions for both TFTs have been described elsewhere[17][62]. Typically TFTs with SiN:H<sub>x</sub> gate dielectric exhibit more stable behaviour in the time scales relevant to this work (as compared to TFTs with PECVD SiO<sub>x</sub> gate dielectric), and thus constitute reference samples for the instability measurements of the SiO<sub>x</sub> TFTs.

Results of constant current biasing of TFTs with SiN:H<sub>x</sub> are shown in Figure 3-16. The graphs show negligible  $\Delta V_T$  in the 25 seconds time window. Using the same set-up, SiO<sub>x</sub> TFTs were subjected to constant current biasing, the result of which is shown in Figure 3-17. After each constant current measurement the TFTs needed to be recovered to their original state, which was achieved by applying a small negative gate voltage of -1V for 50s. The suitability of this biasing condition with respect to device recovery was verified by a number of stress and reset cycles which consistently yielded the same device properties.

Comparison of Figure 3-16 and Figure 3-17 shows a clear abnormality in the behaviour of the TFTs. Furthermore,  $\Delta V_T$  is in the negative direction resulting in an enhancement of the apparent field effect mobility.

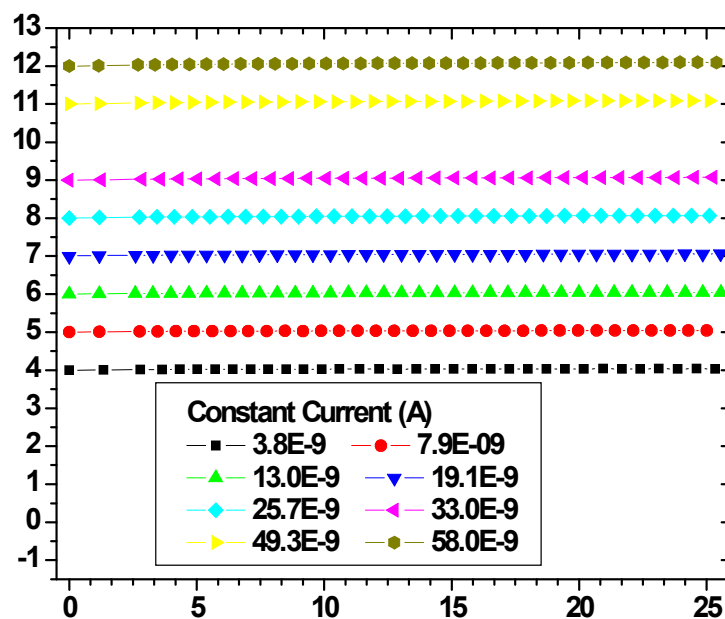


Figure 3-16 Constant current measurement of TFTs with SiN:Hx gate dielectric

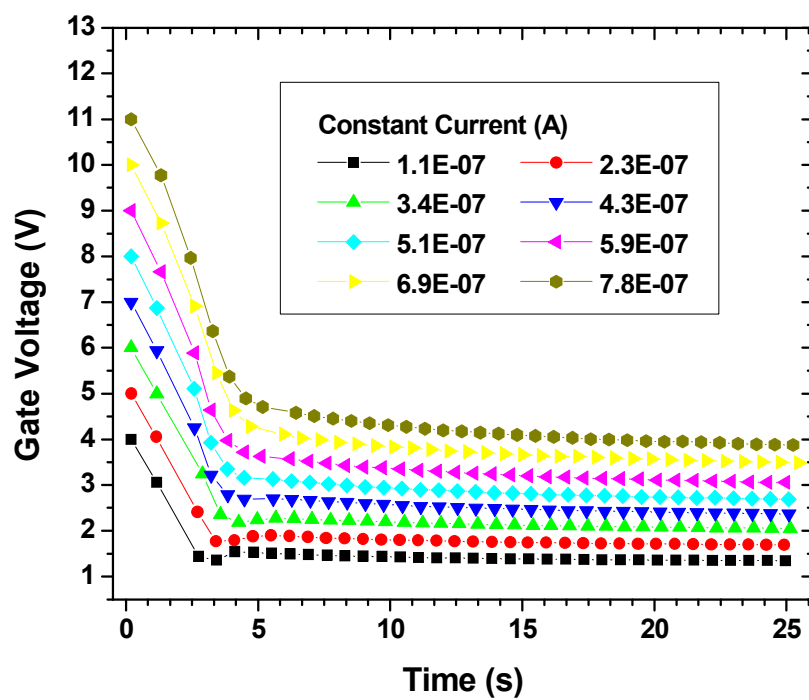
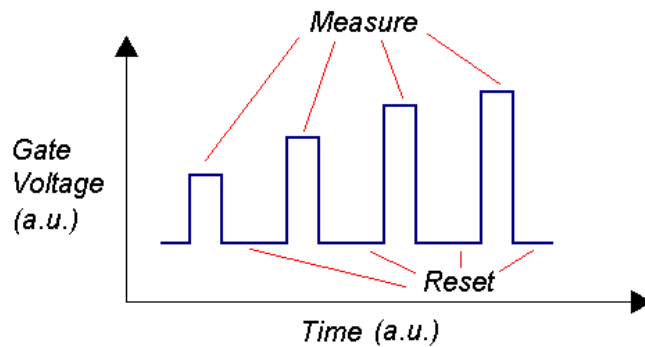


Figure 3-17 Constant current measurement of TFTs with SiOx gate dielectric

To extract the transfer characteristics by compensating for the distortion introduced by the presence of  $\Delta V_T$ , we consider three possible approaches. The first apparent solution is to perform the gate sweep fast enough such that  $\partial V_T \ll \partial V_{GS}$  fulfils the condition for Eqn. (3.16). However, this approach may prove difficult as it is unclear how fast the measurement should be in order to avoid errors induced by  $\Delta V_T$  whilst maintaining the device in the static condition. An alternative approach is to calculate the rate of  $V_T$  shift from Figure 3-17, and substitute this rate into Equation (3.16). However, this is not meaningful because the rate of  $\Delta V_T$  and the dynamic “initial  $V_T$ ” are different for different gate voltages in the voltage sweep mode.

The approach taken in this work allows  $V_T$  to shift and distort the measurement data, as long as the initial  $V_T$  and  $\Delta V_T$  values are the same for all of the data points in the measurement. Here, we have used a 200 ms pulse voltage to turn the device on and measure current. After each pulse we reset the device to a unified state by applying -1V for 50 seconds. Figure 3-18 shows the timing diagram of the voltage applied to the TFTs. It is assumed that with each pulse  $V_T$  is shifted by the same amount. Indeed this corroborates with the observed extrapolated value of  $V_T$  shift for each value of current within this time period.



**Figure 3-18** Timing diagram (not drawn to scale) showing the voltage pulses used to decouple the effect of TFT instability on the transfer characteristics

Figure 3-19 shows the transfer characteristics of a TFT using the standard voltage sweep method and the alternative method reported here. Although a similar value in current is reached in both cases, the  $\Delta V_T$  has the effect of stretching the gate voltage (horizontal) axis. Figure 3-20 shows the transconductance calculated using  $g_m = \partial I_{DS} / \partial V_{GS}$ . Using the standard method leads to an overestimate of the field effect mobility by a factor of nearly 7. Furthermore, the unusually sharp drop in the transconductance when the standard method is used is no longer observed, indicating that this is a feature induced by device instability.

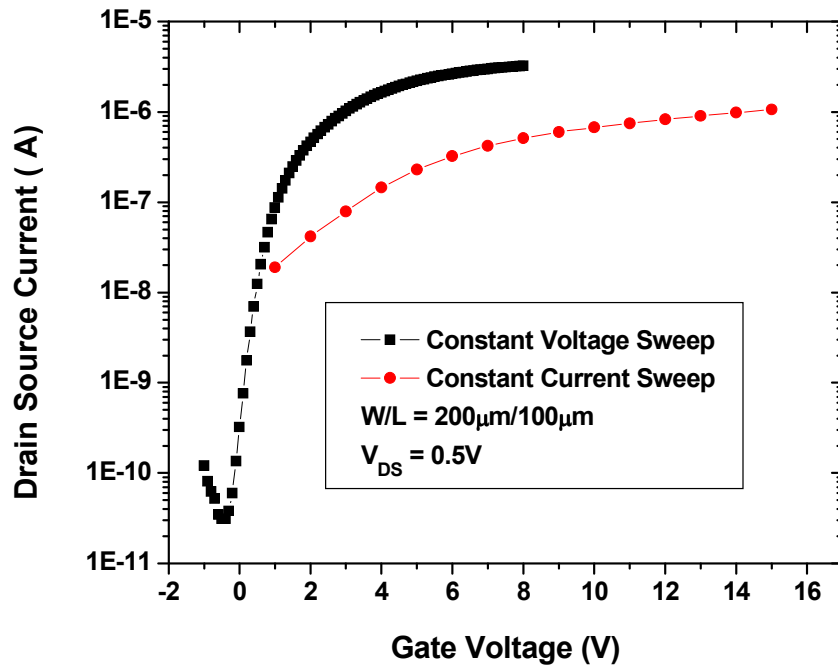


Figure 3-19 Transfer characteristics of SiOx TFTs



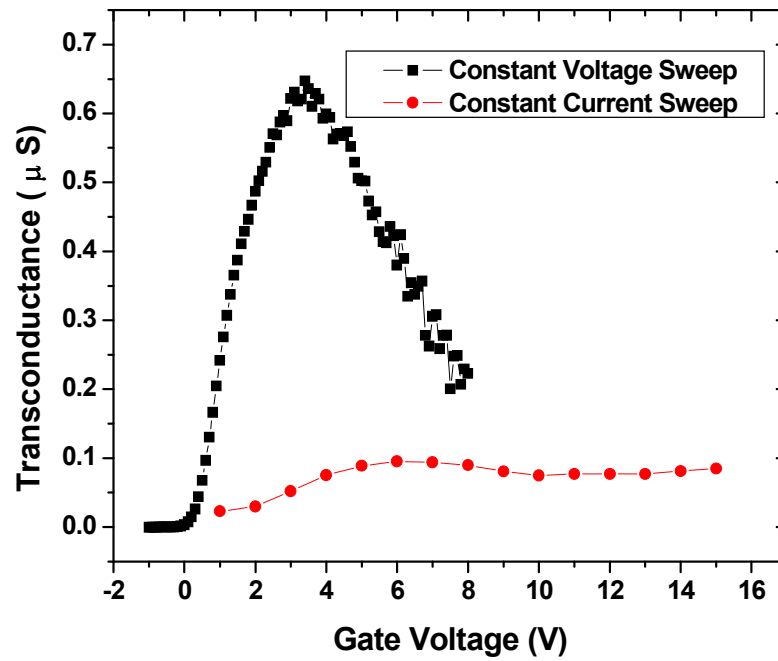
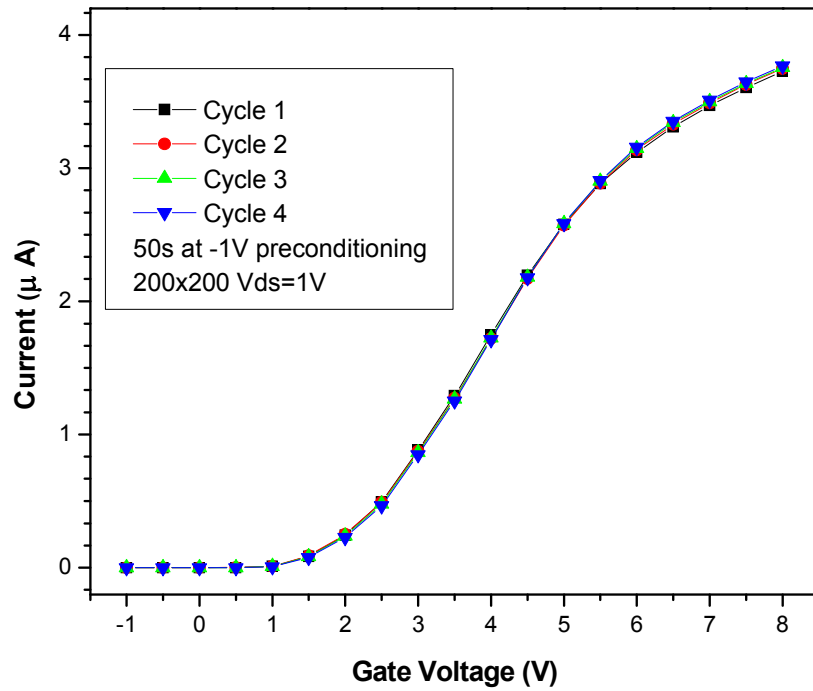


Figure 3-20 Transconductance curves with the conventional and alternative techniques

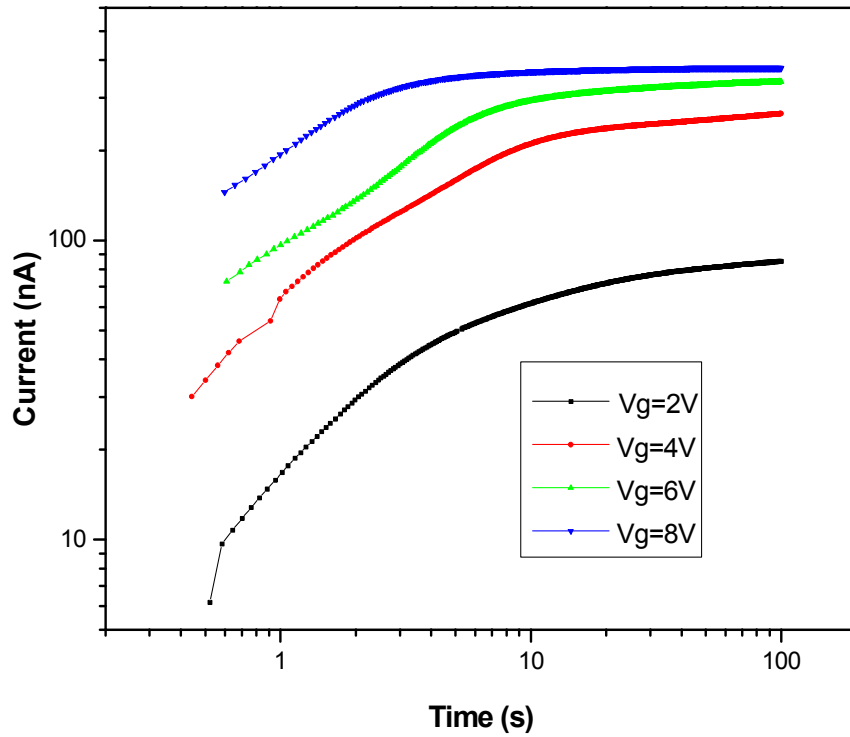
### 3.3.3 Spice Model

Ability to control any instability in the device is critical if it is to be used in a circuit. In the case of dynamic  $V_T$  shift, the  $V_T$  value needs to be restored to a fixed value. This can be achieved by applying a small negative voltage. Figure 3-21 shows that applying a -1V gate voltage for 50s recovers the  $V_T$  shift, resulting in a repeatable transfer curve over a number of cycles.



**Figure 3-21** Resorting  $V_t$  using a gate bias of -1V for 50s

Understanding and modelling of the current-voltage-time characteristics of the device is important for its application in a circuit. Figure 3-22 shows transient behaviour of the TFTs under application of a fixed gate voltage. It should be noted that the device was reset before each measurement using the method described in the previous section. Figure 3-22 shows that transient current behaviour is a combination of a sharp initial rise, and a gradual rise afterwards. Similar dual-rate behaviour has been observed for the  $V_T$  shift related to mobile ion drift and charge polarisation [124] and is due to a self-limiting saturation process.



**Figure 3-22** Current-time characteristics of the TFT under application of a fixed voltage bias

Figure 3-23 shows the equivalent circuit used in the SPICE simulation. A double RC circuit is used to model the dual-rate transient behaviour of the device, with R1C1 representing the initial non-saturated conditions and R2C2 representing the secondary slow  $V_T$  shift. A voltage controlled voltage source (VCVS) is used to emulate the effect of the  $V_T$  shift. Although in this work a simple linear relation is used to relate the output of the VCVS, this can be expanded to represent a more realistic model. The Shichman-Hodges model is used as a simple approximation to describe the FET.

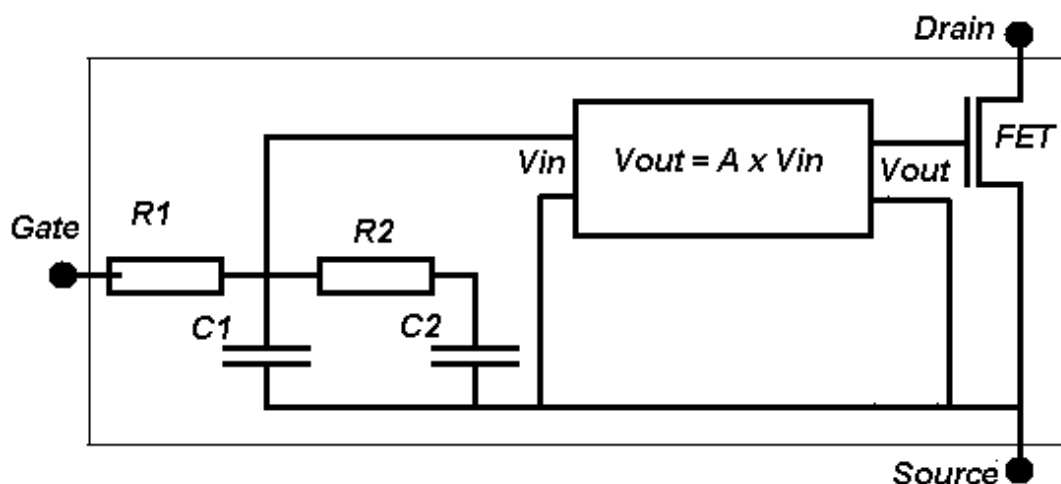
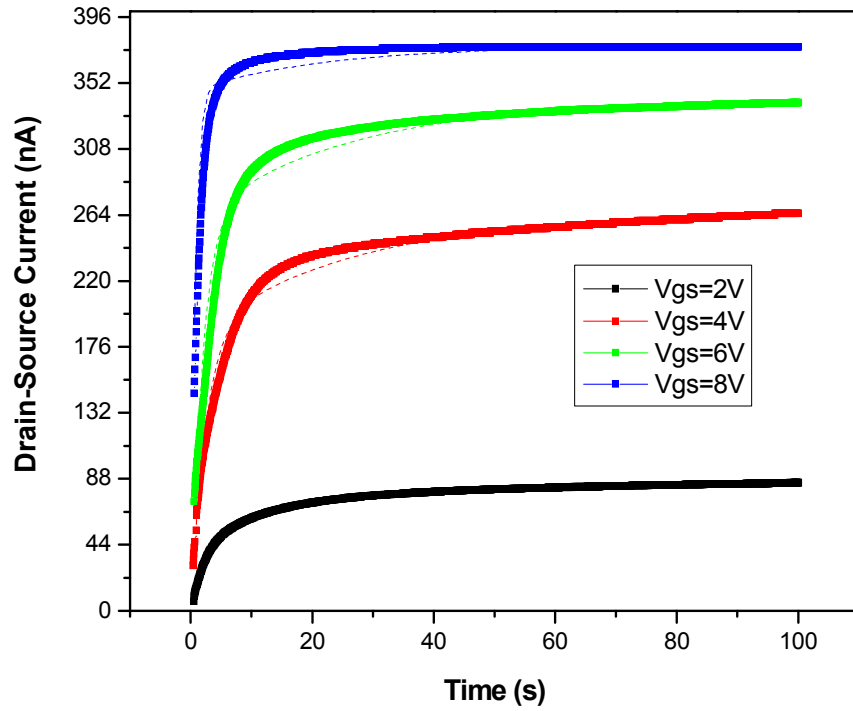


Figure 3-23 Schematic of equivalent circuit for low temperature oxide TFTs implemented in SPICE

Figure 3-24 compares the result of simulation (dotted lines) with the measurement results. An acceptable fit can be achieved using this approach. The fit for each value of gate voltage was achieved by adjusting the values of  $R1$  and  $A$ . Physically,  $R1$  represents the rate of change in  $V_T$  in the non-saturated condition. This rate is a function of  $V_G$  [124][120][121]. The value of  $A$  represents the final shift in the  $V_T$ , which once again is a function of  $V_G$ . However, the value of  $R2$  is maintained; fixed to represent the saturation in  $V_T$  shift rate.



**Figure 3-24** Current-time characteristics of the TFT. Dotted lines show the simulation result

It is difficult to control the turn-off of the TFT using this gate dielectric, resulting in complications in the circuit design stage. Therefore this approach of transconductance is not used in this work.

## 3.4 TFT devices

### 3.4.1 Fabrication Process

A number of TFT device structures and corresponding fabrication processes have been developed. Two broad categories are bottom gated and top gated TFTs. Top gate TFTs are commonly used with a  $\text{SiO}_x$  gate dielectric in combination with  $\mu\text{c}/\text{nc}\text{-Si}$  or poly-Si channels[125]. However  $\text{SiO}_x$  is not suitable for this work due to the process temperature budget [126] and the poor interface with a-Si:H [18][127]. There are two

fabrication processes commonly used for bottom gate TFTs: back channel etch (BCE) and etch stop (ES). The BCE process requires fewer masks and fewer steps. Furthermore self-aligned BCE processes have been demonstrated leading to shorter channel devices [128]. However, despite its advantages the BCE process leads to lower mobility and higher TFT off current due to the defects at the back of the channel and the thicker a-Si:H channel layer [129][130]. Given that low off current is important in this work the ES fabrication process is used.

Figure 3-25 shows the cross sectional diagram of the process flow. The bottom gate inverted-staggered TFT with a SiN:H dielectric structure was used in the work. After a three step solvent cleaning and oxygen plasma etching of any organic contamination layer, the substrate was loaded in a thermal evaporator to evaporate a 50nm layer of Cr (0.1~0.2 nm/s) for the gate electrode (step A). This layer was patterned (step B) and loaded in the PECVD for the deposition of the tri-layer (step C).

The tri-layer consisted of an active channel layer (a-Si:H or nc-Si:H – 50nm) sandwiched between two SiN:H (300nm gate and 150nm passivation) layers. The first SiN:H would serve as the gate dielectric and the second as a passivation nitride and etch stop. The top SiN:H was patterned and etched using buffered HF to open contact areas (step D) before the PECVD deposition of the bi-layer (step E).

The bi-layer consists of a n+ nc-Si:H contact layer (50nm) and a SiN:H (150nm) passivation nitride and was patterned using buffered HF (to etch the SiN:H) and KOH etch to etch the contact and channel layers (step F). A fast HF dip was performed before loading the sample in the PECVD for the deposition of a 150nm SiN:H layer (step G).

The single SiN:H layer was patterned and etched using buffered HF (step H). Before loading the sample in the evaporator for the final metal contact, a quick HF dip was

performed. The contact metal layers 200~300nm evaporated aluminium (~0.5 nm/s) (step I) and patterned and etched using wet aluminium etchant (step J). All of the photolithography steps were performed using MICROPOSIT S1818 Positive Photoresist.

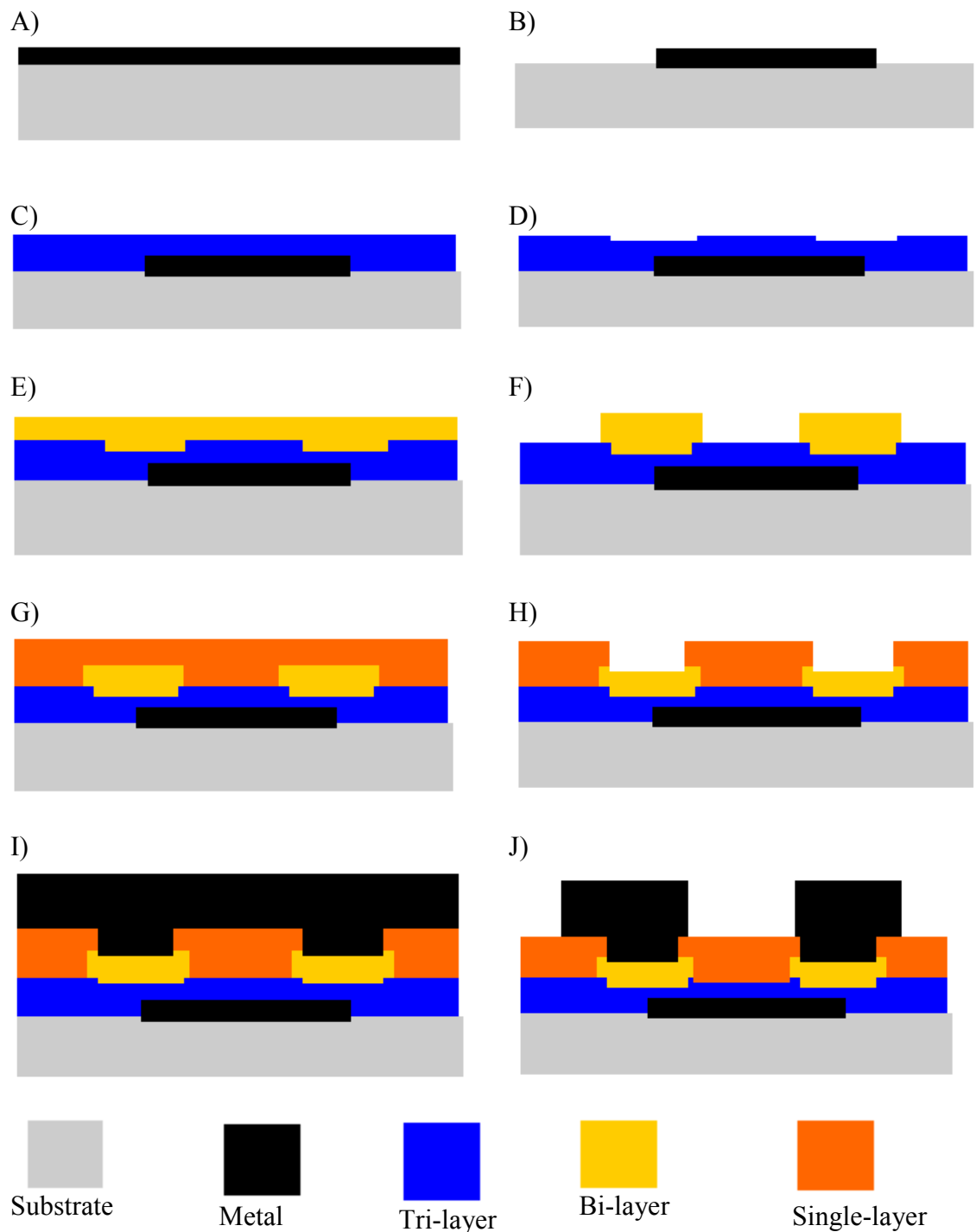
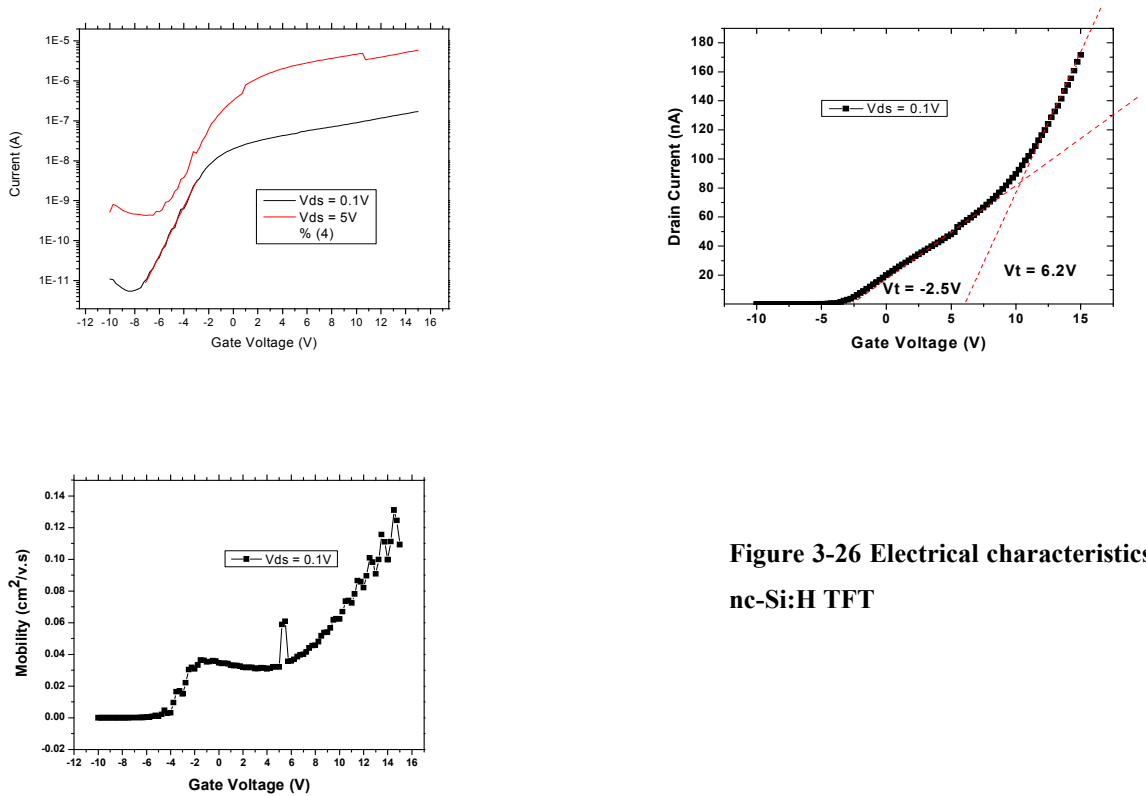


Figure 3-25 TFT process flow diagram

### 3.4.2 Current Voltage Characteristics

Two generations of devices with different channel layers were fabricated and characterised, one using nc-Si:H (50nm) and the other using a-Si:H (50nm). Figure 3-26 shows the transfer characteristics and the linear field effect mobility of the TFT fabricated using the nc-Si:H discussed in 2.4.1. A clear double slope behaviour, resulting in two threshold voltages, can be seen from the linear transfer graph. The TFT has a poor subthreshold slope (1.63 V/dec), and poor mobility ( $0.1 \text{ cm}^2/\text{Vs}$ ) in the measurement range. The device exhibits high off current and poor on/off ratio  $10^5$ .

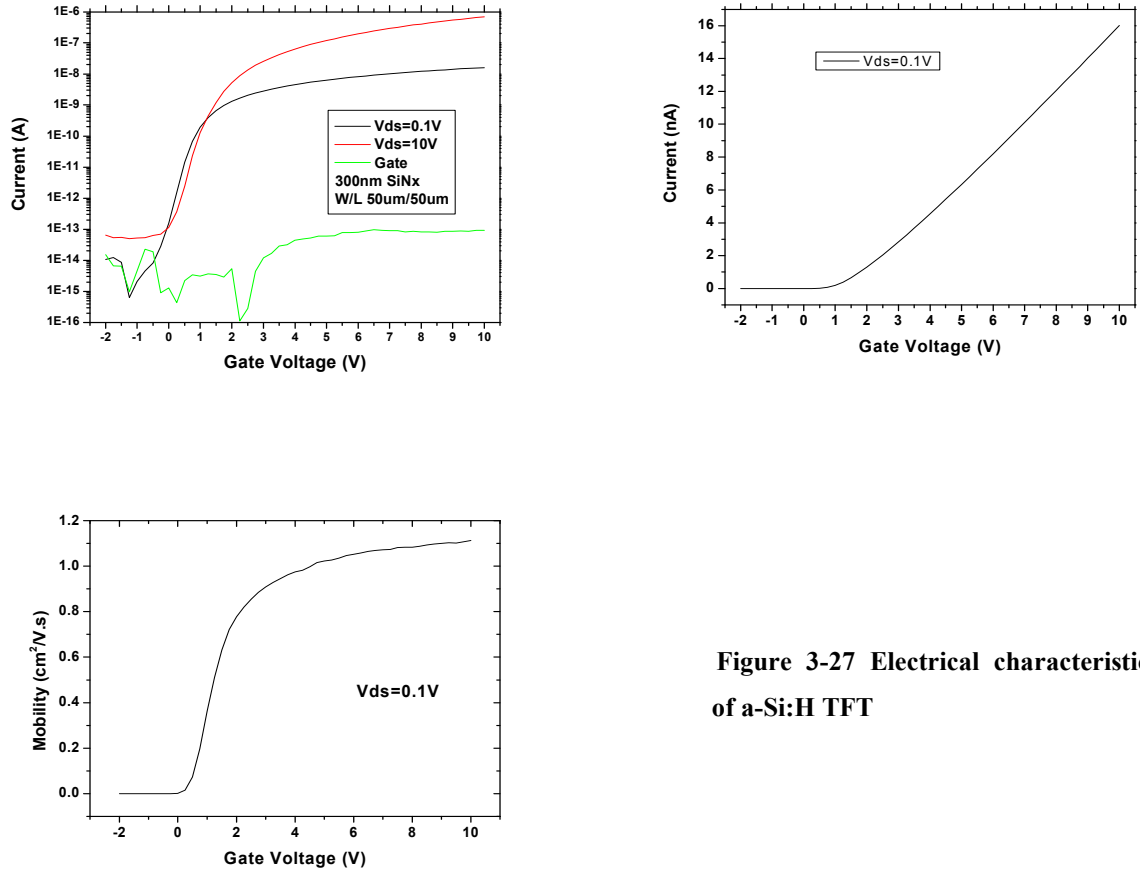


**Figure 3-26 Electrical characteristics of nc-Si:H TFT**

Figure 3-27 shows the transfer characteristics of a TFT fabricated using a good quality a-Si:H channel layer. This channel layer is also used for the fabrication of solar



cells and is discussed in section 2.6.1. The TFT shows an improved performance, with excellent subthreshold voltage slop (0.28V/dec); high linear field effect mobility (1.1  $\text{cm}^2/\text{Vs}$ ); and a low  $V_T$  of 1.8V.



**Figure 3-27 Electrical characteristics of a-Si:H TFT**

The fabrication of good quality a-Si:H TFT suggests that the reason for poor performance of the nc-Si:H TFT is not due to the gate dielectric. The behaviour observed in Figure 3-26 for nc-Si:H is the result of either a defective channel layer, or plasma induced damage to the gate dielectric interface.

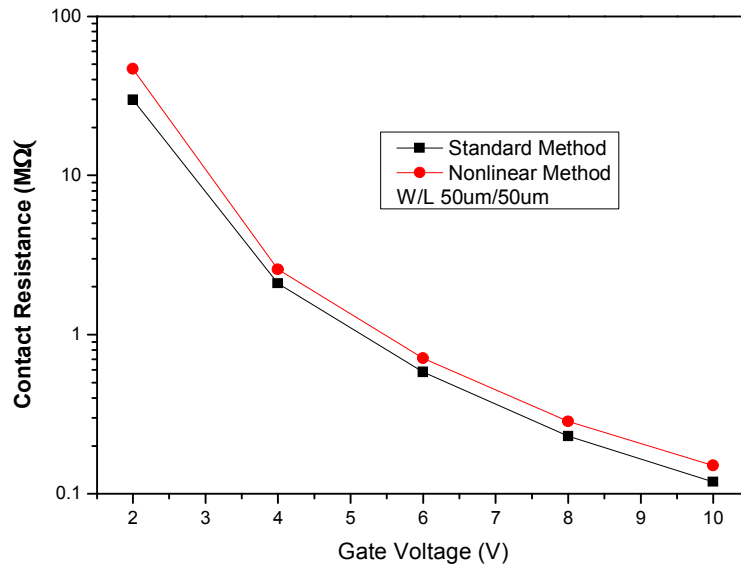
Although a limited electrical characterisation was performed on the nc-Si:H which was consistent with a device quality nc-Si:H, the measurements were not enough to rule out a defective channel layer. This has been shown by Lee et al. [131] who showed that a defective nc-Si:H film (observed in HRTEM, and when used as an absorber layer in p-

i-n) could have comparable electrical and Raman properties to a good quality nc-Si:H. Further material characterisation is needed to establish the underlying reasons for the poor response of the nc-Si:H film.

### 3.4.3 Contact Resistance

Using the method outlined in section 3.2.1 the contact resistance was investigated. The contact resistance was extracted in the linear range ( $V_{ds}$  0.1V to 1V) for devices with channel length of 23 $\mu$ m, 50 $\mu$ m, 80 $\mu$ m and 130 $\mu$ m and channel width of 50 $\mu$ m for a number of gate voltages. Figure 3-28 shows the extracted contact resistance as a function of gate voltage and compared with the values extracted using the standard channel length scaling method. It can be seen that using both methods the contact resistance drops as a function of gate voltage, although using the standard method results in an underestimate of contact resistance.

Contact resistance varies by over 2 orders of magnitude as the gate voltage is swept from 2 to 10V. This clearly shows that the contact resistance is not simply a parasitic constant contact resistance. The total contact resistance per unit width yields 250~1  $\Omega$ -cm as the gate voltage is varied. This compares favourably with devices fabricated using similar deposition techniques at 150°C, where the report value was 230  $\Omega$ -cm [132].



**Figure 3-28 Dependence of contact resistance on gate voltage**

As discussed in section 3.4.1, the interface of the channel/doped layer and the metal/doped layer during the fabrication is exposed to the atmosphere, photoresists, and buffered HF. This may result in contamination at the interfaces. The sources of contamination can be the presence of residues of photoresist (MICROPOSIT REMOVER 1165 was used for removing photoresist), or cross-contamination from other fabrication processes in the cleanroom via the buffered HF.

In addition to contamination, defects are likely to be present at the interfaces. The general assumption is that the HF etching of silicon results in the termination of the surface with hydrogen leading to low density of defects. However, it has been shown that the HF etching of c-Si [133] and a-Si:H [134] surfaces leads to an increase in the surface states density (surface states densities of  $1.5 \times 10^{11} \text{ cm}^{-2}$  to  $6 \times 10^{12} \text{ cm}^{-2}$  have been reported). It has been suggested that this value is highly dependent on the concentration of the HF solution used [135]. However, it should be noted that the doped layer is grown using PECVD plasma which contains a significant amount of atomic hydrogen.

The effect of PECVD plasma on the surface states at the channel/doped layer interface is unclear.

It has been shown that high temperature ( $>180^{\circ}\text{C}$ ) annealing of a-Si:H results in reduction in the defect states [136]. These results have been shown for both post deposition defect creation (SW type defects) [137] and films grown with defects [138]. The reason for annealing has been attributed to the motion of atomic hydrogen in a-Si:H film, leading to the passivation of dangling bonds [139]. Given that the maximum process temperature of  $150^{\circ}\text{C}$  has been used, the dangling bond defects at the interface cannot be fully removed by annealing, leading to the presence of defect states at the interface [140].

#### 3.4.4 Electrical Stress Measurements

The device was stressed in the linear range using a gate voltage of 10V and a drain-source voltage of 0.5V. Stressing of a-Si:H TFTs results in a change in their characteristics via two processes: defect state creation at the channel and/or interface and charge trapping in the dielectrics [141]. The defect states in the channel affect the sub-threshold voltage slope and their creation leads to its degradation [142]. This is accompanied with a shift in the threshold voltage. On the other hand, charge trapping in the dielectric leads to a shift in the threshold voltage without a change in the  $V_T$ . Depending on the stressing voltage, and the quality of channel and dielectric, one of the two processes dominates.

Figure 3-29 shows the results of TFT stressing on the subthreshold voltage slope (SS) and the threshold voltage ( $V_T$ ). It can be seen that the value of  $V_T$  shifts, although the value of SS remains constant, suggesting charge trapping in the silicon nitride is a

dominant mechanism in the device instability. This is consistent with the results shown in section 2.4.2, which suggest a silicon rich silicon-nitride.

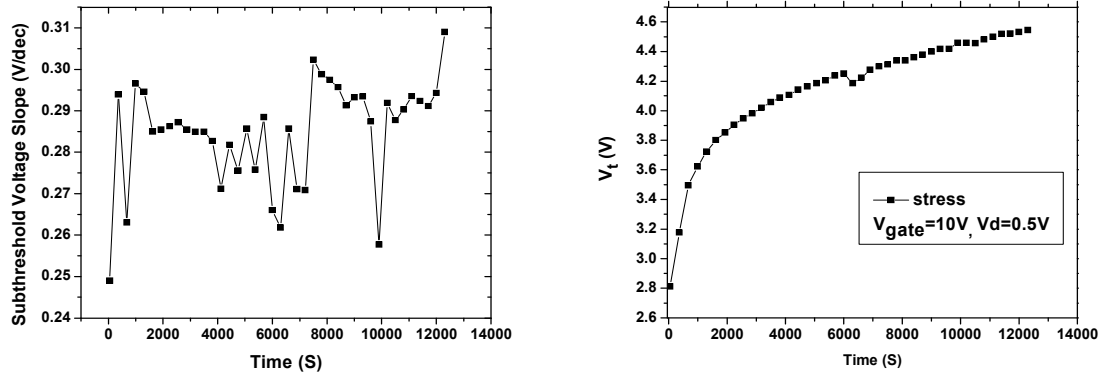


Figure 3-29 Effect of stressing on the subthreshold voltage slop and threshold voltage

### 3.5 Summary and Conclusions

In this chapter the results of the work on thin film transistors were presented. Two sections were presented which outlined possible issues with using low temperature processes. Firstly, contact resistance was discussed and a new parameter extraction method, capable of accounting for both ohmic and non-ohmic components of contact resistance was proposed. An AMPS-1D simulator was used to examine the validity of the proposed extraction method and to compare it with the standard extraction method. It was shown that the contact resistance extracted, using the new approach, matched the true device contact resistance more accurately, when compared with the standard extraction method. The effect of contact resistance on field effect mobility, and its variation with the gate voltage for a number of contact resistance models was investigated. A brief discussion was presented, on a possible physical mechanism for injection resistance (part of the contact resistance) for devices used in this work.

Contact resistance limits the current voltage characteristics of a device and thus its mobility. However, the TFTs' dynamic instability is another low temperature effect which can enhance the device mobility. nc-Si:H top gate TFTs with low temperature silicon oxide gate dielectric, fabricated at the University of Waterloo, were investigated. It was shown that DC transfer measurement results in an anticlockwise hysteresis. This measurement results in a shift in the  $V_T$  in a direction away from the gate voltage (i.e. towards higher negative voltages, when applying positive gate voltages) and thus an enhancement in the transconductance. The physical origin of this effect was attributed to the movement of mobile ions in the gate dielectric (or polarisation of dipoles).

A new measurement method was developed which allowed the decoupling of the transient and static behaviour of the device, and allowed the extraction of the true field effect mobility. Although a method of "resetting the  $V_T$ " was demonstrated, it was concluded that due to the poor control of the off state, such a device would not be suitable for use in a simple circuit.

Two sets of devices were fabricated, one using nc-Si:H as the channel layer and the other using a-Si:H. The same SiN:H was used for both devices as the gate dielectric and passivation layer. Although the nc-Si:H TFTs showed poor performance (high SS, high  $V_T$ , low mobility), the ones using a-Si:H showed excellent performance. The poor performance of the nc-Si:H TFTs was attributed to either a plasma damaged SiN:H/nc-Si:H interface or a low quality nc-Si:H film. Further material characterisation (e.g. HTEM and the Hall-effect mobility) can be performed to establish the quality of the nc-Si:H with more confidence. The issue of gate dielectric/channel interface can be verified by fabricating top gate TFTs using the same nc-Si:H channel.

a-Si:H TFT was selected for this work. Contact resistance was extracted using the channel length scaling method and the non-linear method. As expected, the standard method resulted in an underestimate of the contact resistance (by 56% for small gate voltage and 22% for the highest gate voltage). The value of contact resistance was dependent on the gate voltage, which could be due to the presence of defects at the a-Si:H/n<sup>+</sup>nc-Si:H interface.

The device was stressed under electrical bias and it was shown that the dominant mechanism of the instability was charge trapping in the dielectric. This was expected as the SiN:H used in this work was not nitrogen rich. This can be rectified by adjusting the gas ratio of SiH<sub>4</sub>/NH<sub>3</sub>. However, this approach was not taken in this work: unstable TFTs were used for the circuit to allow the investigation of TFT instability on the circuit behaviour.

Parameter	This work	120°C a-Si:H TFT on plastic substrate (etch stopper process) [143].	150°C TFT on polyimide foil (back channel etch process) [144].	150°C a-Si:H TFT on plastic substrate (back channel etch process) [145].
<i>Field Effect Mobility (cm<sup>2</sup>/V.s)</i>	1.1	0.8	0.5	0.4
<i>Subthreshold Voltage (V/dec)</i>	0.28	0.5	N/A	0.82
<i>Threshold Voltage (V)</i>	1.8	2.3	3.5	1.5
<i>On/Off ratio</i>	10 <sup>6</sup>	10 <sup>5</sup>	10 <sup>7</sup>	10 <sup>6</sup>

**Table 3-1 Comparison of a-Si:H TFTs fabricated in this work with devices fabricated at similar deposition temperatures**

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## 4 Solar Cell

### 4.1 Introduction

#### 4.1.1 P-i-n Solar Cell Operation

Figure 4-1 shows the basic cross sectional diagram of a p-i-n solar cell and the corresponding simplified band diagram (short circuit condition). Absorbed photons generate electron-hole pairs which are then separated by the inbuilt potential of the p-i-n junction, leading to the drift of electrons to the n-layer and holes to the p-layer. Useful absorption only takes place in the i-layer.

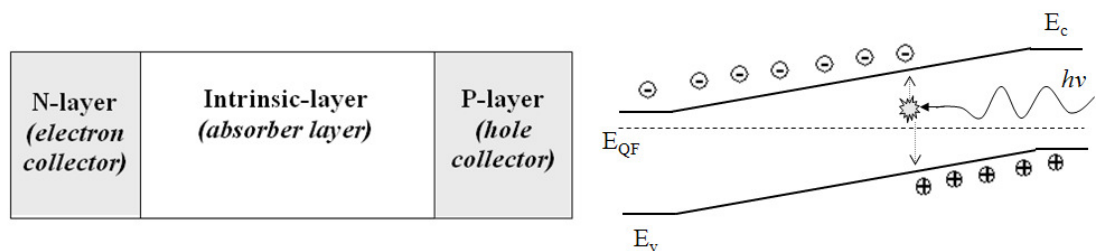
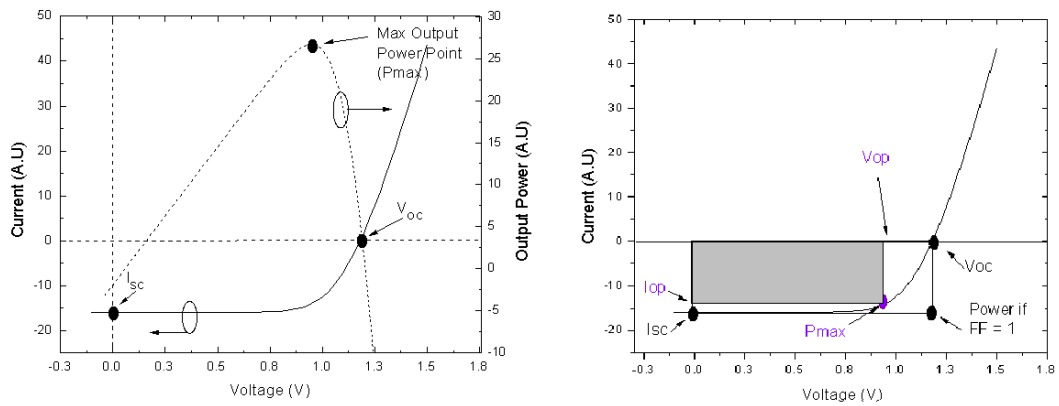


Figure 4-1 P-i-n cross section diagram

The solar cell operates by providing both voltage and current to a resistive load and thus generates power. Under a constant light intensity, the device's output voltage and current depend on the resistivity of the load. As shown in Figure 4-2, changing the value of the resistor (and thus the solar cell's operating point) leads to a change in the output power of solar cell. The operation in maximum power point is achieved by adjusting the

load resistance such that the solar cell is generating its maximum power ( $P_{\max}$ ). The efficiency of the solar cell is the ratio of electrical power at the maximum power point to the incident light power.

The solar cell's efficiency is related to three parameters routinely used in device characterisation: open circuit voltage ( $V_{OC}$ ), short circuit current ( $I_{SC}$ ) and the fill factor (FF). Figure 4-2 shows the current-voltage characteristics of a typical solar cell and the locations of  $I_{SC}$  and  $V_{OC}$  on the graph. This diagram also shows the maximum power point's voltage ( $V_{op}$ ) and current ( $I_{op}$ ). The purple rectangle represents the maximum output power ( $P_{\max}$ ). Fill factor is defined as the ratio of the purple rectangular area to the white rectangular area.



**Figure 4-2 Current-voltage characteristics of a typical solar cell showing  $V_{OC}$ ,  $I_{SC}$  and maximum operating point (purple)**

The relationship between FF and the  $P_{\max}$  is given in the following equation (4.1):

$$FF = \frac{V_{OP} \times I_{OP}}{V_{OC} \times I_{SC}} = \frac{P_{Max}}{V_{OC} \times I_{SC}} \quad (4.1)$$

Therefore an alternative way of looking at the efficiency,  $\eta$ , is

$$\eta = \frac{P_{Max}}{P_{Light}} = \frac{V_{OC} \times FF \times I_{SC}}{P_{Light}} \quad (4.2)$$

The highest efficiency is achieved when the values of FF,  $I_{SC}$ , and  $V_{OC}$  are maximised. A number of physical mechanisms can affect FF,  $I_{SC}$ , and  $V_{OC}$ . Depending on the operating regime of the device these physical mechanisms can dominate different cell parameters. For a good quality solar cell, illuminated under standard light, the following approximation can be used as indicators [146]:

- Wavelength independent FF is significantly influenced by parasitic shunt and series resistances. These parasitic resistances do not affect the  $V_{oc}$  and  $I_{sc}$  points.
- $V_{OC}$  is related to the built-in potential and any recombination current strongly reduces it. It is also related to the bandgap of the material used (e.g. c-Si has lower  $V_{OC}$  compared with a-Si:H).
- $I_{SC}$  is a function of the electron-hole pair generation rate in the i-layer and is strongly affected by the photon management approach.

A number of steps can be taken to improve solar cell efficiency. They can be grouped in three general categories:

1. Connecting to cells (e.g. metallisation layers and electrical connections) to improve fill factor:
  - High conductivity electrodes and contacts to minimise series resistance (10 Ohms/sq sheet resistances for TCO electrodes, better for metal electrodes).

- Optimise process to maximise shunt resistance.

2. Avoiding loss in the generated photocarriers:

- Good p/i and n/i interfaces (e.g. using graded layers, avoid dopant diffusion).
- Reduce defect density in the i-layer.
- i-layer thickness appropriate for the mobility-lifetime product (200~300 nm for holes in a-Si:H).

3. Maximising the generation of the photocarriers:

- Light trapping: reduce reflection at air/device interface and maximise the reflection at the back reflector (e.g. Al, Ag which have a good reflectivity).
- Reduce the absorption in p, n and electrode layers. Thin, wide bandgap p-layer (p-layer bandgap of above 2eV when used in a-Si:H solar cell) is typically used in combination with transparent conductive oxide (TCO).
- Sufficient i-layer thickness.
- Use i-layer(s) that absorb light across solar spectrum (e.g. tandem cell).

As Figure 4-3 left shows, a-Si:H does not absorb most of the light below 1.7eV (above 720nm, approximately bandgap of a-Si:H). Comparing this with the solar spectrum (1.5AM), Figure 4-4, shows a significant portion (48%) of sunlight is above 720nm which would not be absorbed by a-Si:H. This is a significant disadvantage of a-Si:H solar cells. Tandem

cells (e.g. a-Si:H/uc-Si or a-Si:H/a-SiGe:H) have been used to improve the IR response of a-Si:H solar cells. Figure 4-3 top, shows the quantum efficiency of a tandem cell with 3 absorber layers (a-Si:H and a-SiGe:H with different germanium concentrations leading to different band gaps). It can be seen that the PV response extends to over 950nm, resulting in increased  $I_{sc}$ .

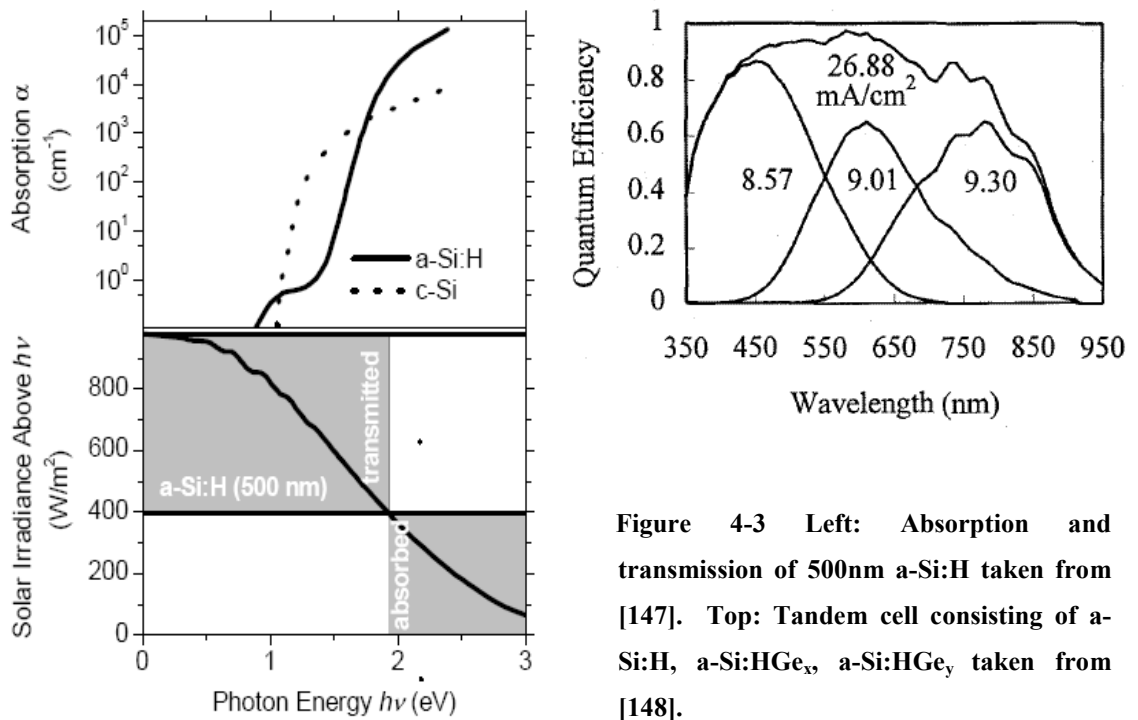


Figure 4-3 Left: Absorption and transmission of 500nm a-Si:H taken from [147]. Top: Tandem cell consisting of a-Si:H, a-Si:HGe<sub>x</sub>, a-Si:HGe<sub>y</sub> taken from [148].

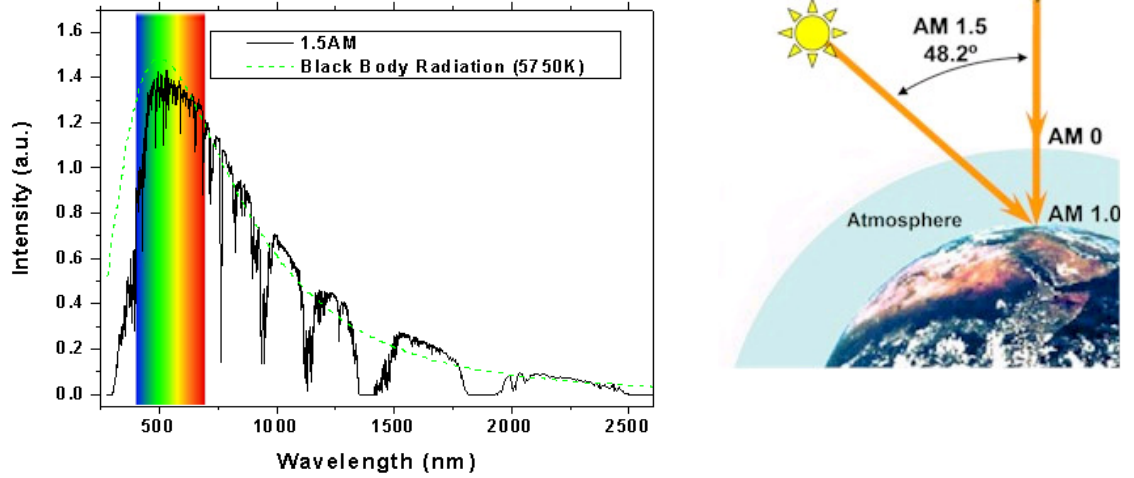


Figure 4-4 1.5 AM solar radiation compared with 5750K black body radiation. Solar spectrum taken from [149]

#### 4.1.2 Device Configuration

Depending on the order of deposition of the n, i and p-layers the solar cell can have one of the two general structures shown in Figure 4-5: substrate structure (n-i-p) or superstrate structure (p-i-n). Given that in a-Si:H the mobility-lifetime product of the holes is less than electrons,<sup>6</sup> the cells should be designed such that the light is absorbed and thus the electron-hole pair is generated close to the hole collection electrode, (i.e. p-layer). Therefore, the window layer is generally p-doped, allowing for more efficient hole collection in a-Si:H. This approach is adopted in this work.

As shown in Figure 4-5, in addition to the n, p and i-layers, additional films are needed for the fabrication of solar cells. Indium tin oxide (ITO) or other transparent

<sup>6</sup> The actual values of mobility vary depending on the experimental method used. However, the value of hole mobility has been consistently lower (by around one order of magnitude) than that of electrons. For example values of  $2\text{cm}^2/\text{V.s}$  and  $0.1\text{ cm}^2/\text{V.s}$  for electrons and holes respectively had been reported for room temperature drift mobility using time of flight measurement [150].

conductive oxides (TCO) are used as the contact electrode on the window side of the device, window contact. Aluminium or silver are commonly used as back contacts due to their high reflectivity, thus increasing light absorption in the i-layer.

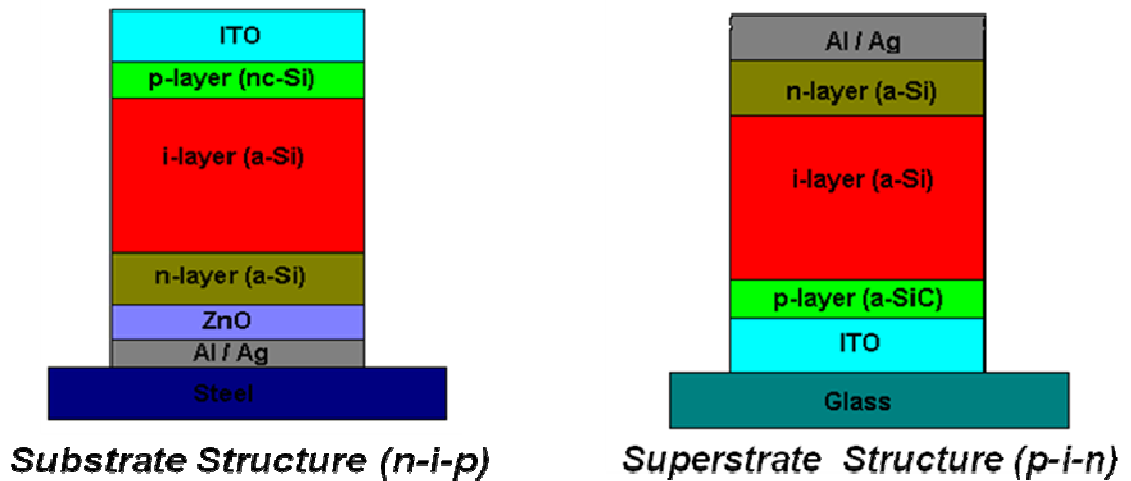


Figure 4-5 Cross sectional diagram of two possible solar cell configurations

An additional TCO layer is placed between the n-layer and the back contact metal layer. ZnO is used in Figure 4-5 as an example of such a layer. ZnO's role is to prevent metal diffusion in a-Si:H, whilst providing a transparent and conductive interface between the back contact metal and the n-layer. The diffusion of metal results in the creation of traps and recombination centres [151], and subsequent degradation of the solar cell. Using TCO between the n-layer and the back reflector helps to extend the operating life of the *superstrate structure* [151]. However, the back contact TCO is essential for a *substrate structure*, as that metal/silicon junction would be exposed to temperatures of at least 200°C when the a-Si:H is deposited [152]. In this work cells are deposited at low temperatures and it is important to verify the need for the diffusion barrier layer when using the substrate structure (n-i-p). Assuming that the diffusion of the metal obeys Fick's law:

$$n(x, t) = n(0) \cdot \operatorname{erfc} \left[ \frac{d}{\sqrt{4Dt}} \right] \quad (4.3)$$

$n(0)$  is the atomic density of the source material assumed  $10^{23}/\text{cm}^3$  for Al;  $d$  is the distance from the source material and  $t$  is the time.  $D$  is the diffusion constant. At  $150^\circ\text{C}$  substrate temperature, a diffusion constant in the range of  $10^{-15} \sim 10^{-16} \text{ cm}^2/\text{sec}$  for Al and Ag has been reported [153]. Table 1-1 summarises the normalised density,  $n(x,t)/n(0)$ , of the Al (or Ag) after 30min of  $150^\circ\text{C}$  heating at two different depths (20nm and 40nm). It suggests that heating the sample for 30min at  $150^\circ\text{C}$  would result in a significant diffusion of metal in a-Si:H film, which may lead to degradation of the device. This demonstrates the need for a diffusion barrier when using the n-i-p structure, even at low deposition temperatures.

<b>N(x,t)/n(0)</b>	<b>Depth (nm)</b>	
<b>Diffusion rate (<math>\text{cm}^2/\text{s}</math>)</b>	<b>20</b>	<b>40</b>
<b><math>10^{-15}</math></b>	0.291	0.035
<b><math>10^{-16}</math></b>	0.00086	$10^{-11}$

**Table 4-1 Normalised density of defused Ag (Al) at 20nm and 40nm depths in silicon film. The values are for 30min at  $150^\circ\text{C}$ .**

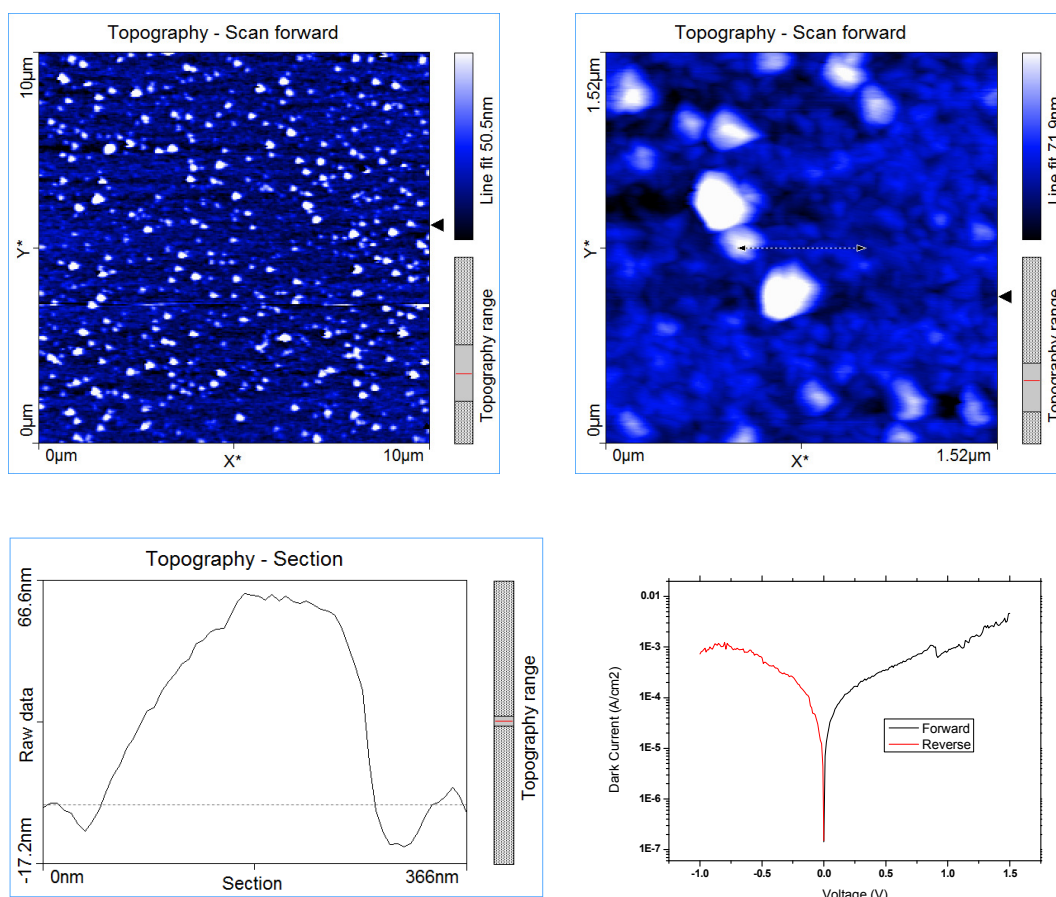
In addition to metal diffusion, high deposition temperature can also result in the formation of hillocks in aluminium [154] and subsequent shunting of the p-i-n devices. This appears to be the case particularly for evaporated aluminium which suffers from higher stress.<sup>7</sup> Figure 4-6 shows the AFM image on the glass/Al/ITO surface. 200nm aluminium was evaporated followed by 8nm ITO sputtering at an elevated temperature.

<sup>7</sup> Sputtered aluminium has been used directly (i.e. without TCO) for the fabrication of p-i-n devices. (e.g. Pimentel et. al. 2009 [155]).



This appears to have resulted in the formation of hillocks on the Al film with features 60~70nm high and 200~300nm diameter. The Al/ITO layers were deposited at MVSystems Inc., Colorado.

A high quality a-Si p-i-n was deposited on the Al/ITO at 150°C. A semi-transparent gold electrode was evaporated as the final contact. The device's I-V characteristic is shown in Figure 4-6. It shows very poor performance and almost no rectification (same p-i-n recipe on ITO coated glass results in close to  $10^7$  rectification ratio).



**Figure 4-6 AFM on glass/Al (200nm)/ITO (8nm) multilayer. ITO was sputtered at 100C. Bottom right: dark current-voltage characteristics of a p-i-n diode deposited on the substrate.**

It has been suggested that aluminium interacts with n-type a-Si:H, either by counter-doping via the defect generation process [156] or by reduction in its effective thickness

[157]. Both of these processes result in diminishing the n-layer in the p-i-n device, and a subsequent reduction in diode properties. Alternatively hillock formation and damage to the p-i-n structure could result in poor diode characteristics.

The solution to the hillocks and diffusion problem is the use of thicker TCO. Alternatively metals such as chromium can be used as the back contact. Diffusion of Cr in a-Si:H is slow and limited to a few nm due to the formation of Cr silicide, which acts as a barrier layer against further Cr diffusion [158]. However, Cr has a lower reflectivity compared with Al or Ag leading to a reduction in the back reflected photons and subsequently lower  $I_{sc}$ .

TCO is also used as the window electrode. An alternative to this is a semi-transparent metal layer. Gold is a good candidate due to its high conductivity. Thin evaporated gold on silicon has a high resistivity (due to the formation of small grains [159]) and poor adhesion. For this, a titanium adhesion layer was selected which forms a smooth interface with silicon (due to its reaction with native oxide) and lower resistivity Ti/Au [160].

2nm (at rate of  $\sim 0.01\text{nm/s}$ ) titanium and 15nm (at rate of  $\sim 0.1\text{nm/s}$ ) gold was evaporated using e-beam evaporation on to a glass substrate. The film showed sheet resistivity of  $13\ \Omega/\text{sq}$ , as measured using a 4 point probe measurement.

Figure 4-7 shows the transmission spectrum through the Ti/Au multilayer film. It shows the peak transmission of 47% at 520nm with transmission in the blue (400nm) of

32% and red (650nm) 38%.<sup>8</sup> Therefore, the use of a thin Ti/Au layer in place of TCO results in significant optical losses and therefore a reduction in the  $I_{sc}$ .

The substrate structure (n-i-p) is compatible with non-transparent substrates and this allows for a more flexible approach to system design. However, as was shown, the substrate structure without the use of TCO (i.e. using Cr as the back reflector and Au/Ti as the window electrode) would result in a significant reduction in the efficiency. In addition to the  $I_{sc}$  the type of electrodes may result in a change in the diode's built-in potential and thus  $V_{oc}$ . However, this problem is a minor issue and can be overcome by using thick enough doped layers [161].

When using the superstrate structure, transmission through the substrate should also be considered. A PEN substrate has about 90% transmission in the visible range; similar to that of glass (Corning Eagle 2000 used in this work has 92% transmission). Due to the unavailability of TCO deposition tools, the superstrate structure on glass substrate with commercial ITO is selected for this work. The commercial glass coated ITO used was from the Cando Corp. (Taiwan). The ITO had a sheet resistivity of  $\sim 10 \Omega/\text{sq}$  and no significant absorption in the visible range.

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<sup>8</sup> Gold is known for having high reflectivity in the red/IR range, which is consistent with low transmission at longer wavelengths. At shorter wavelengths of blue and UV, gold shows a high absorption, consistent with the drop in the transmission below  $\sim 500\text{nm}$ . The combination of strong absorption in the blue and strong reflection in the red results in a blue-green range. See Otto Loebich's Gold Bulletin 5,1,2 (1972).

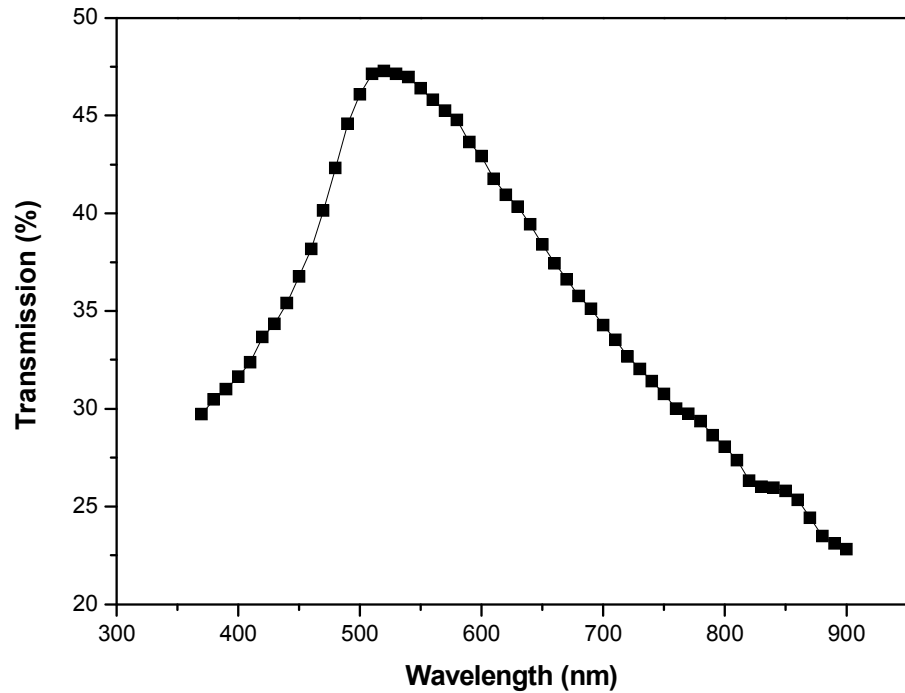


Figure 4-7 Transmission spectrum of Ti(2nm)/Au(15nm) on glass

## 4.2 P-i-n Devices

### 4.2.1 Fabrication Process

Solar cells were fabricated using a maximum process temperature of 150°C on ITO coated glass with a sheet resistivity of 10  $\Omega$ /sq. After solvent cleaning steps, the sample was loaded in the PECVD for the deposition of the p type a-SiC:H (15nm), intrinsic a-Si:H (300nm) and n type nc-Si:H (50nm) using the deposition conditions described earlier. After the deposition the sample was transferred to the load-lock and was allowed to cool down over a 30~45min period. A layer of aluminium (200~300nm) was evaporated (thermal evaporator with pressure of better than  $10^{-6}$  Torr) through shadow masks to define the solar area. Finally, a 1min RIE etch (using SF<sub>6</sub>) over the entire area was performed to remove the highly conductive n-type nc-Si:H layer and possibility the

top surface of the intrinsic a-Si:H. Aluminium contact pads acted as the etch mask. The cells had various sizes although in this work the cell area is  $0.04\text{cm}^2$ .

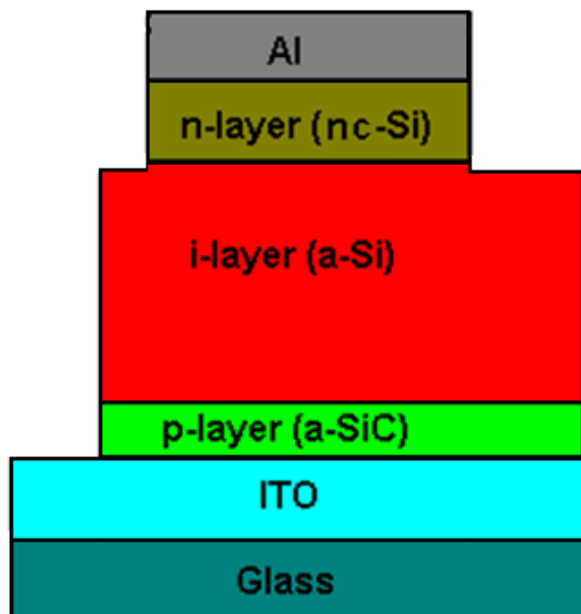


Figure 4-8 Solar cell cross sectional device

#### 4.2.2 Cleaning Process Optimisation

The effects of boron cross contamination in the i-layer when fabricating p-i-n devices in a single chamber PECVD system is well known and investigated. This typically results in the reduction of collection efficiency under blue light.

The cleaning step adopted in here consisted of etching the chamber wall with  $\text{CF}_6 + \text{O}_2$  cleaning gas and a 2min purge of the chamber with  $\text{H}_2$  and  $\text{N}_2$  gas. Identical structures with different etch times were fabricated. The effect of the etch time on the device was tested by investigating the collection efficiency for different wavelengths. For this, the current was measured at 0V and -1V. The ratio of the two values of the current is plotted in Figure 4-9.

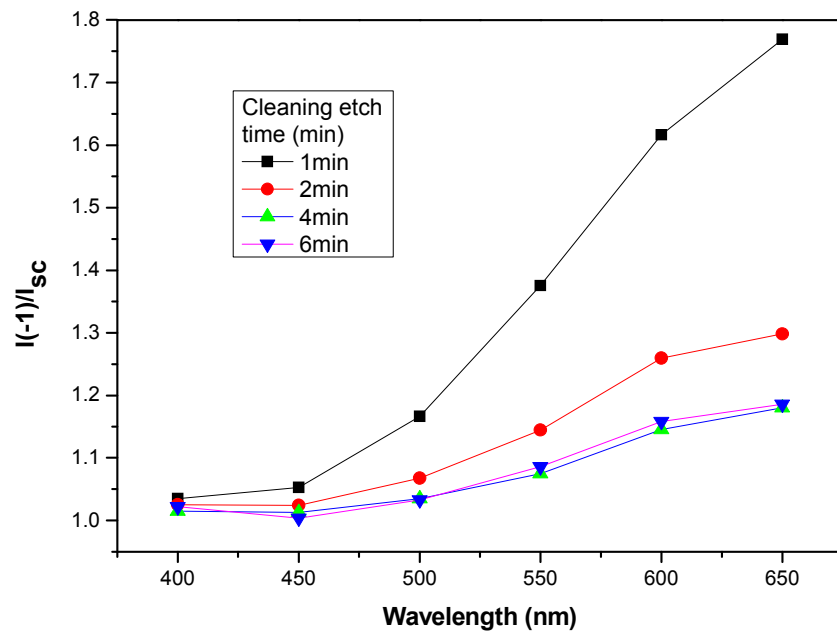


Figure 4-9 Effect of CF<sub>4</sub> and O<sub>2</sub> cleaning process on the carrier losses

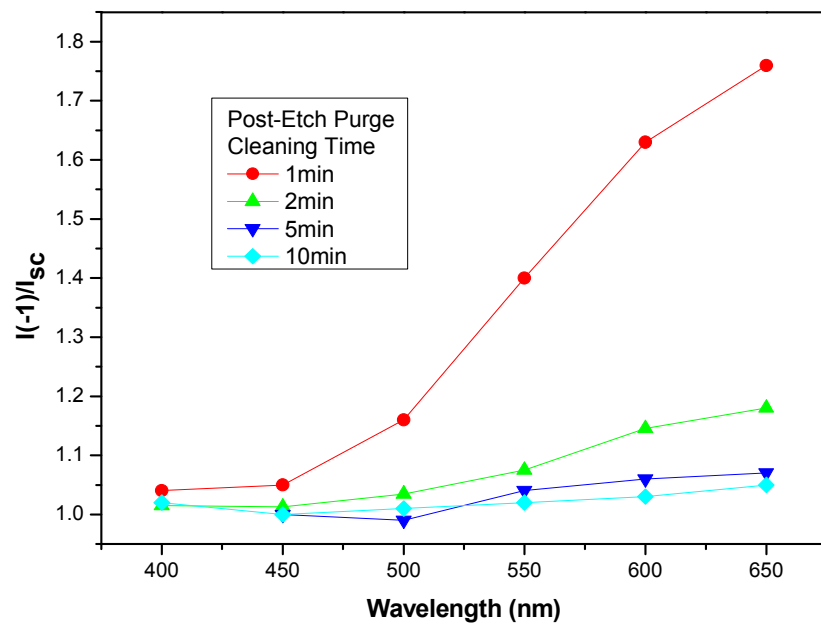


Figure 4-10 Effect of the post cleaning purge on the collection efficiency

It can be seen that the cleaning process results in an improvement in the carrier collection in the red. Similar improvements in the carrier collection have been reported in the devices fabricated in single chamber systems. However they have been reported for shorter wavelengths (blue) as the cross-contamination takes place in between the i and p-layers. In the PECVD system used in this work (with a dedicated intrinsic chamber) cross contamination takes place between the n and p-layers. It has been suggested that doping of a-Si:H with phosphorous and boron results in the creation of boron-phosphorous clusters [162], leading to lower doping efficiency [163], as well as an increase in the defects for a non-optimised film [164].

After 4min of cleaning, the value of  $I(-1)/I_{sc}$  drops to 1.18 and no further improvement is made. 1.18 is still high compared with the blue wavelengths, suggesting that there is still some inefficiency in the collection which could be due to contamination from the cleaning gases themselves. This is further investigated by looking at the effect of the post-cleaning purge on the collection efficiency as shown in Figure 4-10. It shows an improvement in the collection efficiency when the post-cleaning purge, in excess of 5min, is used where the red  $I(-1)/I_{sc}$  (650nm) drops to 1.05. This is consistent with the result of the work reported by U.S. Graf (2005) which is summarised in Table 4-2 [165]. Although U.S. Graf used a  $SiH_4$  plasma and not a gas purge in her work, they both appear to have a similar effects. In this work a cleaning etch time of 6min and a purge of 10min is used.

treatment	state	V <sub>oc</sub> [mV]	σ <sub>std</sub>	FF	σ <sub>std</sub>	J <sub>sc</sub> [mA/cm <sup>2</sup> ]	η [%]	σ <sub>std</sub>
CO <sub>2</sub> (30min.)	initial	447	9	0.525	0.053	18.2	4.27	0.47
	annealed	450	12	0.419	0.059	17.5	3.30	0.54
	regenerated	414	18	0.378	0.045	18.7	2.94	0.44
a-Si :H	initial	395	18	0.495	0.022	10.9	2.12	0.19
	annealed	318	69	0.450	0.010	8.5	1.21	0.28
	regenerated	403	30	0.517	0.043	15.7	3.28	0.51
SF <sub>6</sub> /O <sub>2</sub>	initial	481	11	0.456	0.011	11.8	2.58	0.06
	annealed	467	19	0.420	0.006	13.7	2.69	0.10
	regenerated	355	6	0.395	0.004	13.0	1.83	0.04
<i>SF<sub>6</sub>/O<sub>2</sub></i> & <i>a-Si :H</i>	initial	491	7	0.614	0.005	18.2	5.48	0.09
	annealed	<b>516</b>	<b>4</b>	<b>0.675</b>	<b>0.008</b>	<b>18.5</b>	<b>6.44</b>	<b>0.06</b>
	regenerated	492	7	0.609	0.015	18.3	5.48	0.16

Table 4-2 Effect of chamber treatment on uc-Si superstrate structure taken from [165].

### 4.2.3 Spectral Characteristics

Figure 4-11 shows the V<sub>oc</sub> vs I<sub>sc</sub> for red (650nm) and blue (450nm) wavelengths. Under illumination the p-i-n current-voltage behaviour can be described by Eqs (4.4) where J<sub>L</sub> is the current density under illumination, J<sub>sc</sub> is the short circuit current density, J<sub>0</sub> is the reverse saturation current density, and KT/q is 25.8mV at room temperature. n is the diode quality factor, which is governed by the diode's carrier recombination mechanism.

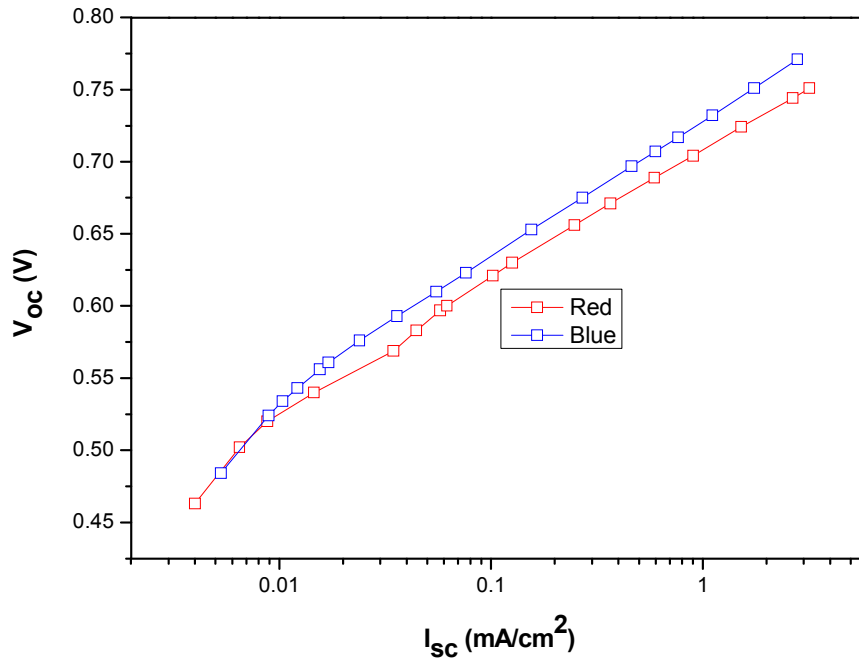
$$J_L = J_{sc} - J_0 \left( \exp \left( \frac{qV}{nKT} \right) - 1 \right) \quad (4.4)$$

Under open-circuit conditions the above equation simplifies to:

$$0 = J_{sc} - J_0 \exp \left( \frac{qV}{nKT} \right) \rightarrow J_{sc} = J_0 \exp \left( \frac{qV_{oc}}{nKT} \right) \quad (4.5)$$

Therefore the slope and offset of the ln(J<sub>sc</sub>) vs V<sub>oc</sub> yields n and J<sub>0</sub>.





**Figure 4-11  $I_{sc}$  -  $V_{oc}$  of the p-i-n device obtained by varying light intensity**

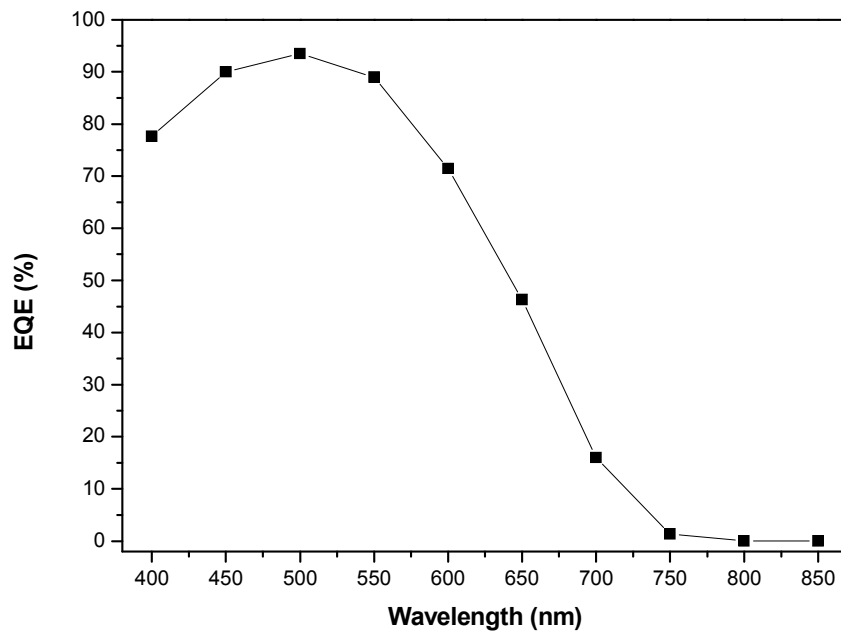
Red (1.32  $\mu\text{m}$  penetration depth) has a uniform absorption in the p-i-n whereas blue is absorbed within the first 50nm. Under red illumination, electron-hole pairs are generated throughout the i-layer. Under blue illumination the electron-hole pairs are only generated close to the p/i interface. Figure 4-11 shows the following:

- At low light intensity blue and red responses merge. This suggests that the p/i interface dominates recombination at low light intensities.
- At high light intensity, closer to the PV operating point, red and blue responses diverge with a higher  $V_{oc}$  in the blue. This indicates the presence of losses due to i-layer recombination.

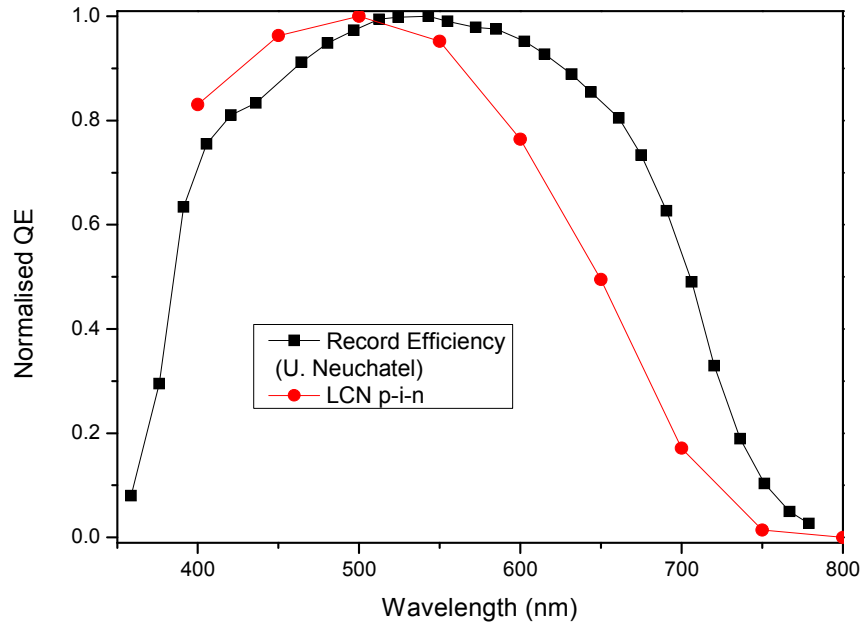
This suggests that both processes are present, although the i-layer recombination dominates at higher currents.

The spectral response of a solar cell device is a useful tool for investigating the relative change in the photo-carrier collection at different wavelengths.

Figure 4-12 shows the external quantum efficiency (EQE) graph of a device fabricated in this work. It can be seen that the solar cell has a good response in the blue range, due to the thin p-layer. However, the response in the red is very poor. Figure 4-13 compares the normalised spectral response of the solar cell fabricated in this work and the one with the highest efficiency reported (which uses a textured substrate combined with an anti-reflective coating [96]). As expected it shows that the LCN device has a much worse response in the red than the University of Neuchatel device.



**Figure 4-12 Spectral response of solar cell device**



**Figure 4-13 Normalised EQE of the p-i-n fabricated in this work and p-i-n with record efficiency. U. Neuchatel data taken from [96].**

#### 4.2.4 Dark Current-Voltage Characteristics

Dark current-voltage characterisation is a powerful tool for investigating properties of p-i-n diodes and by extension p-i-n solar cells. It has been shown that the PV characteristics such as  $V_{OC}$  or FF are related to the dark current-voltage characteristics [166]. Recombination in the bulk and interfaces affects the dark I-V and solar cell properties.

The current-voltage characteristics have transient and steady state components. The transient effects are the result of charge trapping and detrapping and can be significant at low current levels. Steady state effects, which are investigated in this section, are the result of recombination and diffusion/drift of the carrier.

For the correct analysis it is critical to decouple the transient and steady state effects by selecting an appropriate measurement time setting. In this work a number of

measurements with different time settings were performed. It was noted that faster measurements resulted in a notable deviation from the slower measurements in the low current range. However, slow measurements with different time settings were similar to each other.

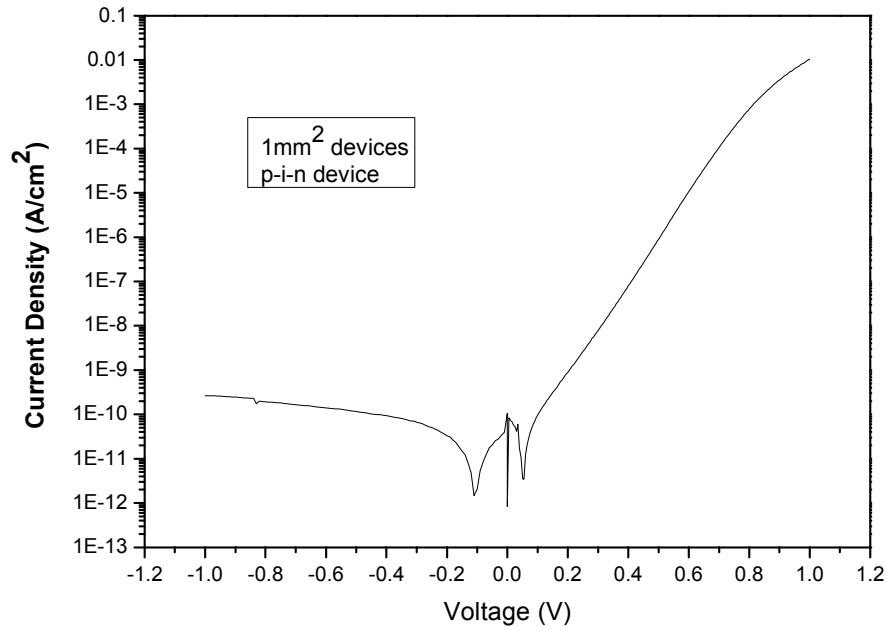
In this work, forward and reverse I-V were measured separately. For both forward and reverse,<sup>9</sup> the measurement started at zero (300s hold time) and voltage was increased in steps of 5mV with the hold time of 10s before each current reading. To avoid the effect of short due to micro-structural defects, measurement was done on small devices ( $0.01\text{cm}^2$ ), and the high conductivity nc-Si:H n-layer was etched using a RIE etch process. No defects were observed under the microscope.

Figure 4-14 shows the dark current-voltage characteristics. Abnormal behaviour in the small voltage ( $-0.1 > 0 > 0.1$ ) is the result of transient effects and is neglected. An ohmic limited I-V characteristic can be seen at the large positive voltages (Voltage  $> 0.8\text{V}$ ).

The reverse leakage at  $-1\text{V}$  is  $300\text{pA}/\text{cm}^2$ . This is over one order of magnitude larger than the state of art p-i-n photodiodes ( $\sim 10\text{pA}/\text{cm}^2$ ). Furthermore, the reverse leakage current does not appear to saturate within the measurement range. The diode ideality factor ( $n$ ) of  $1.549 \pm 0.003$  and the reverse saturation current density of  $5.024 \pm 0.118 \text{pA}/\text{cm}^2$  is extracted in the voltage range of  $0.4 \sim 0.7\text{V}$ .

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<sup>9</sup> It has been suggested [John G. Shaw, 1991] that for a-Si:H the trapping time is shorter than the detrapping time.



**Figure 4-14 Dark current-voltage characteristics**

In a high quality p-i-n diode, high leakage current is generally attributed to a high recombination rate. This recombination has been attributed to either the bulk i-layer or the p/i interface [166]. Another indicator of current transport in a p-i-n is the diode quality factor ( $n$ ). The recombination dominated by the p/i interface results in unity quality factor [167]. However, for recombination in the i-layer, assuming an exponential distribution of density of states, results in an exponential I-V characteristic is outlined below [168]:

$$J_D = J_0 \text{Exp} \left( \frac{qV}{nKT} \right) \quad (4.6)$$

where  $n$  is a temperature dependent value. Only a truly exponential distribution of gap states in a-Si:H results in voltage independent quality factor. The value of  $n$  is inversely related to the rate of the rise in the density of states when moving from the mid-gap to tail states (i.e. the slower the rate of the rise results in a larger  $n$ ).

Deng and Wronski (2005) have used the voltage dependent quality factor as a method of differentiating between the p/i and i-layer recombination [167]. Figure 4-15 shows the dependence of  $n$  on voltage extracted from Figure 4-14. Figure 4-15 shows that  $n(V)$  reaches a localised minimum value of 1.56 at voltage of 0.53V. Comparing this value with the minimum  $n(V)$  value of 1.4 obtained by Deng and Wronski (2005) suggests a slower rise in the density of states in the i-layer and a lower quality i-layer.

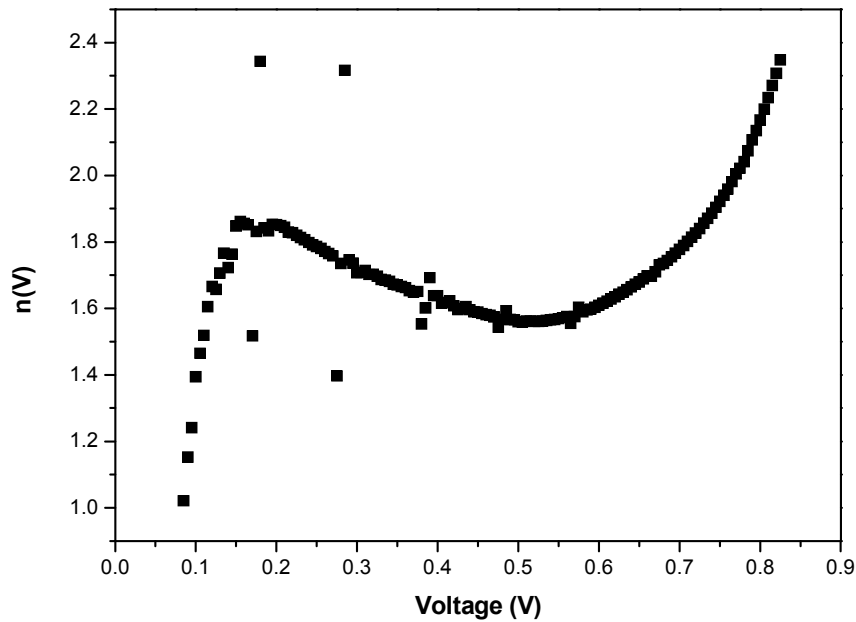


Figure 4-15 Differential diode quality factor extracted from Figure 4-14

Although Deng and Wronski's (2005) method is useful for comparing samples, the dark I-V measurement depends on measurement time settings (e.g. transient currents), and device fabrication (e.g. series resistance). In the following section the current-voltage under light bias is investigated, and provides a more complete picture to allow characterisation of the p-i-n with better certainty.

#### 4.2.5 Light Current-Voltage Characteristics

Figure 4-16 shows the current-voltage characteristics of a p-i-n device under illumination. The measurement was performed using a solar simulator (Oriel class A solar simulator) with the output intensity of  $100\text{mW/cm}^2$  and 1.5AM spectrum. Before the measurement the intensity was confirmed using a calibrated photo-detector.

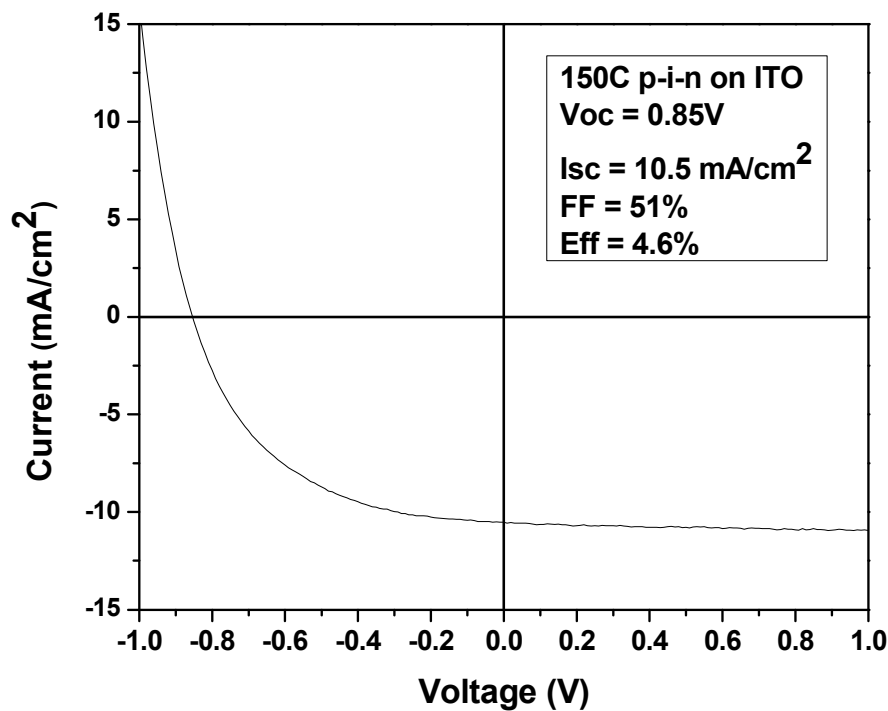


Figure 4-16 Current voltage characteristics under illumination.

### 4.3 Summary and Conclusions

In this chapter the work on individual solar cells is presented. It was shown that without the use of a sputtering system, a superstrate configuration (p-i-n) is a more suitable device configuration.

Boron-phosphorus cross contamination in the doped chamber was identified as a possible source of photo-carrier loss in the device. A suitable cleaning process was developed to minimise any losses.

Using these films and optimised fabrication processes, a solar cell was fabricated and characterised. Table 4-3 compares the performance of the solar cells fabricated in this work with that of reported devices fabricated at similar deposition temperature.

<i>Parameter</i>	<i>This work</i>	<i>150°C a-Si:H p-i-n on PET substrate [169]</i>	<i>150°C a-Si:H p-i-n on PEN (glass)[170]</i>	<i>200°C a-Si:H p-i-n on PEN [171]</i>
Efficiency (%)	4.6%	5.03	3.99 (4.7)	8.8
$I_{sc}(mA/cm^2)$	10.5	11.2	8.4 (9.84)	14.3
FF (%)	51	54.2	61.5 (61.7)	70
$V_{oc}(V)$	0.85	0.83	0.773 (0.774)	0.888

**Table 4-3 Comparison of solar cells fabricated in this work with devices fabricated at similar deposition temperatures**



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## 5 System Design

### 5.1 Circuit Design Approach

As discussed in section 1.2, the thin film supercapacitor (SC) is an alternative candidate to batteries when used as an intermediary energy storage for mobile energy harvesting systems. Use of a SC allows for less stringent circuit requirements, thus making circuit implementation using TFTs a viable option.

The power conditioning circuit considered in this section fulfils two roles:

- Limit the charging voltage: minimum charging voltage and over charging voltage are more flexible in a SC compared to batteries. Nevertheless high charging voltage should be prevented as it results in the SC breakdown [172]. Furthermore, a limited range of voltages supplied to the SC (intermediate energy storage) allows for a more flexible design in the subsequent stages.
- Provides input impedance for the PV array such that it would operate at its maximum power point. The ideal maximum power point tracking system (MPPT) would maintain the PV array at its maximum operating point over a range of illumination intensities, load conditions, ambient temperatures, and PV array lifetime.

Generally, a power conditioning circuit has been implemented using two sub-systems: DC-DC convertor and MPPT. In this work, an attempt has been made to design a circuit which fulfils both functions.

DC-DC convertors have been used to control the output voltage of PV arrays [173]. Switch mode DC-DC convertors are an efficient type of convertor with conversion efficiency of over 95% [174]. Although switch mode convertors using inductors have been widely used, thin film inductors are inefficient due to the planar design and the need for exotic materials [175]. Therefore an inductor-less convertor is more suitable for this work.

Linear regulators are inductor-less DC-DC convertors. A transistor in parallel with the PV array can be used to provide a shunt path across the energy storage unit. In the shunting configuration, the transistor diverts power from the energy storage unit once the SC exceeds the safe operating voltage. Due to the power dissipation in the transistor, this approach can only be used for low power PV arrays [176]. Despite the shunt regulator's simplicity, it suffers from low conversion efficiency. The maximum theoretical average-efficiency of a shunt regulator depends on the input voltage's variation [177]. Generally a BJT has been used as the shunt transistor [178][179]. However, in this work a TFT combined with a suitable circuit is used.

## 5.2 Circuit Design Principles

### 5.2.1 Circuit Description

Figure 5-1 shows the schematic of the charging circuit used in this work. The circuit input would be connected to the PV array and the output to the load capacitor. Transistor  $T_3$  provides the shunt path which acts as an overvoltage protection

mechanism for the capacitor. Transistor  $T_4$  (with  $T_3$ ) sets the output voltage. It also prevents the discharge of the capacitor, via the PV array.

Initially the load capacitor is fully discharged ( $V_{\text{out}} = 0$ ). Connecting the PV array (under illumination) results in the charging of the load capacitor. This leads to an increase in  $V_{\text{out}}$  accompanied with a rise in  $V_{\text{in}}$ . Increase in  $V_{\text{in}}$  results in two things:

- Shift in the PV array's operating point towards higher voltages (and lower currents).
- Higher  $V_{\text{control}}$  leading to higher conduction in the shunt TFT ( $T_3$ ).

As charging progresses, in a correctly designed system, the circuit finally reaches a point where  $T_3$  conducts all of the current, and  $V_{\text{out}}$  reaches a maximum value. This value of  $V_{\text{out}}$  can be chosen to be the maximum voltage the capacitor can reach without any damage. A correctly designed system would act in two ways:

- Limit the variation in the PV array's operating point, allowing it to maintain operation close to the maximum power point.
- Minimise the shunt conduction in  $T_3$  until it is required.

The rest of this section discusses the dependence of output on input voltage (light intensity) and stress. Possible approaches to improve efficiency are considered.

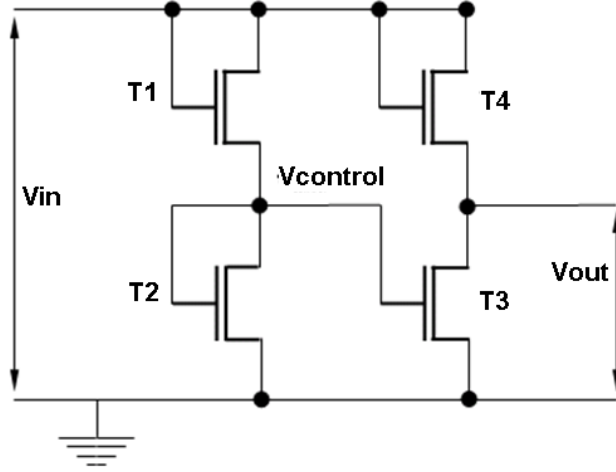


Figure 5-1 Circuit schematic

### 5.2.2 Output Voltage Control

Devices  $T_1$ ,  $T_2$ , and  $T_4$  have their gate and drain connected and therefore they are either in saturation or switched off. The behaviour of the TFT device operating in this range can be approximated as following [180]:

$$I_{DS} \approx K(V_{GS} - V_T)^2 \quad (5.1)$$

where  $K$  is the transconductance and depends on device geometry and channel mobility. Neglecting the gate current, the following equations can be written for the  $T_1/T_2$  branch:

$$I_{DS_1} = I_{DS_2} \approx K_1 \times (V_1 - V_T)^2 = K_2 \times (V_2 - V_T)^2 \quad (5.2)$$

$$K_1(V_{in} - V_{control} - V_T)^2 = K_2(V_{control} - V_T)^2 \quad (5.3)$$

$$V_{control} = \frac{V_{in} - 2V_T}{\left[ \frac{\sqrt{K_2}}{\sqrt{K_1}} + 1 \right]} + V_T \quad (5.4)$$

These are based on the assumption that  $V_T$  is the same for devices located next to each other. This assumption has been used for a-Si:H devices due to the homogeneity of the channel and dielectric [181]. It will be shown later in this section that it is desirable to set  $\frac{\sqrt{K_2}}{\sqrt{K_1}} + 1 \approx 1$ . This would lead to  $V_{control} \approx V_{in} - V_T$ . When overvoltage protection is needed, the capacitive load is fully charged and is no longer drawing significant current. Assuming transistor  $T_3$  operates in the saturation mode (i.e.  $V_{in} - 2V_T < V_{out}$ ) the following equations can be written:

$$I_{DS_3} = I_{DS_4} \approx K_3 \times (V_{control} - V_T)^2 = K_4 \times (V_4 - V_T)^2 \quad (5.5)$$

$$K_3(V_{control} - V_T)^2 = K_4(V_{in} - V_{out} - V_T)^2 \quad (5.6)$$

$$V_{out} = V_{in} - V_T - \frac{V_{in} - 2V_T}{\frac{\sqrt{K_4}}{\sqrt{K_3}} \left[ \frac{\sqrt{K_2}}{\sqrt{K_1}} + 1 \right]} \quad (5.7)$$

The above equation can be simplified by defining  $\alpha = \frac{\sqrt{K_4}}{\sqrt{K_3}} \left[ \frac{\sqrt{K_2}}{\sqrt{K_1}} + 1 \right]$ , rearranging to:

$$V_{out} = \left[ 1 - \frac{1}{\alpha} \right] V_{in} - \left[ 1 - \frac{2}{\alpha} \right] V_T \quad (5.8)$$

when  $\frac{\sqrt{K_2}}{\sqrt{K_1}} \ll 1$ , and  $\alpha$  can be simplified to  $\alpha \approx \frac{\sqrt{K_4}}{\sqrt{K_3}}$ . Using this approach the values

of  $K_3$  and  $K_4$  (and thus  $\alpha$ ) can be adjusted to obtain the desired circuit properties. By

selecting  $\frac{\sqrt{K_4}}{\sqrt{K_3}} = 1$ , the following relation can be written:

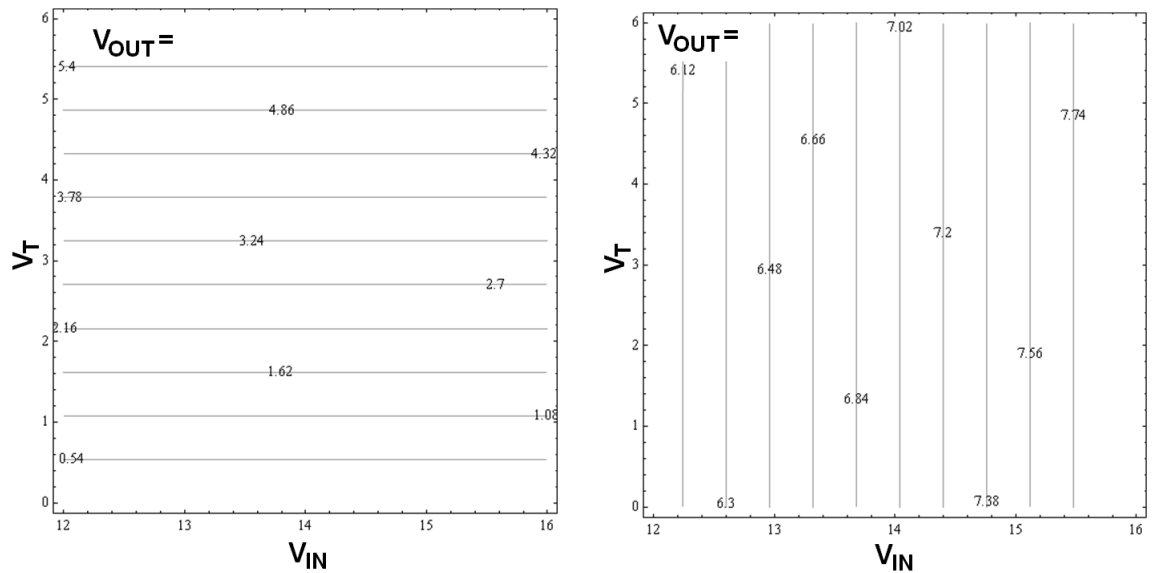
$$V_{out} = \left[1 - \frac{1}{1}\right] V_{in} - \left[1 - \frac{2}{1}\right] V_T = V_T \quad (5.9)$$

This would make  $V_{out}$  independent of light intensity variations and subsequent variations in  $V_{in}$ , making it suitable for use with highly stable TFTs. Alternatively, when

$\frac{\sqrt{K_4}}{\sqrt{K_3}} = 2$ , the following relation can be derived:

$$V_{out} = \left[1 - \frac{1}{1}\right] V_{in} - \left[1 - \frac{2}{2}\right] V_T = 0.5 V_{in} \quad (5.10)$$

making  $V_{out}$  independent of any TFT instability, at the expense of dependency on the light intensity variations. Figure 5-2 shows changes in the value of  $V_{out}$  with variations in  $V_{in}$  and  $V_T$  for  $\alpha = 1$  and 2.



**Figure 5-2 Dependence of  $V_{out}$  on  $V_{in}$  and  $V_T$  for  $\alpha = 1$ , left, and  $\alpha = 2$ , right**

Complete dependence of  $V_{out}$  on either  $V_T$  or  $V_{in}$  is undesirable.  $V_T$  shifts during the circuit lifetime, and  $V_{in}$  is light intensity dependent and would change with the time of

the day and year. As the value of  $\alpha$  increases from 1, the dependency of  $V_{out}$  on  $V_T$  reduces at the expense of  $V_{in}$  dependency. A compromise can be made when choosing  $\alpha$  to increase the stability of  $V_{out}$  for various, realistic, light intensities and over the circuit operation. Furthermore, choosing  $\alpha$  would allow using the circuit design to control  $V_{out}$ . The graph below shows the dependence of  $V_{out}$  to  $V_{in}$  and  $V_T$  for  $\alpha = 1.5$ . It can be seen that now  $V_{out}$  changes with both  $V_{in}$  and  $V_T$ , although to a lesser degree.

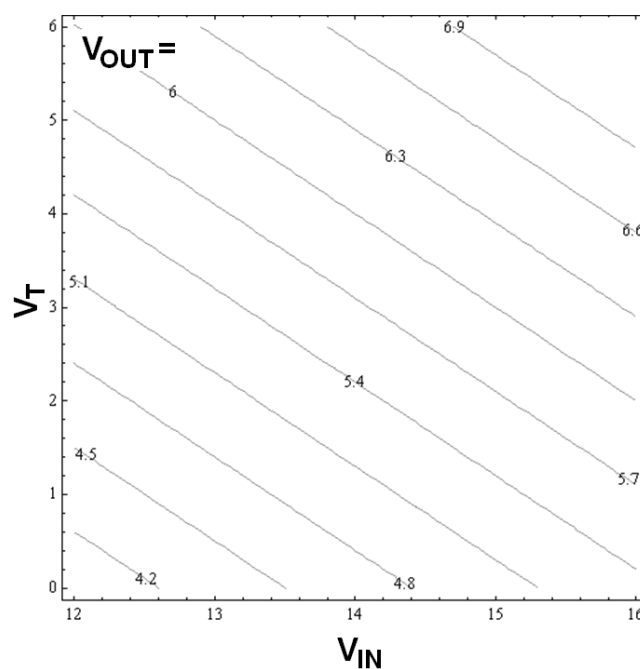


Figure 5-3 Dependence of  $V_{out}$  on  $V_{in}$  and  $V_T$  for  $\alpha = 1.5$

As can be seen in Table 5-1, depending on the stability of the TFTs and the variation in the light intensity, a compromise can be made when selecting  $\alpha$ .

$\alpha = 1.2$ $\Delta V_{out} = 0.17\Delta V_{in}$ $\Delta V_{out} = 0.67\Delta V_T$	$\alpha = 1.8$ $\Delta V_{out} = 0.44\Delta V_{in}$ $\Delta V_{out} = 0.11\Delta V_T$
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Table 5-1 Effect of  $\alpha$  value on change of  $V_{out}$  with variation in  $V_{in}$  and  $V_T$



Up to this point it has been assumed that  $T_3$  operates in the saturation regime. This requires  $V_{in} - 2V_T < V_{out}$ . Substituting saturation condition in equation (4.8) leads to:

$$V_{in} - 2V_T < \left[1 - \frac{1}{\alpha}\right] V_{in} - \left[1 - \frac{2}{\alpha}\right] V_T \quad (5.11)$$

$$\frac{V_{in}}{V_T} < 2 + \alpha \quad (5.12)$$

Equation (5.8) is only valid for a limited voltage input, and it is important to consider the effect of the  $T_3$  operation in linear range. This would lead to the following relations:

$$I_{DS_3} = I_{DS_4} \approx K_3 \times (V_{control} - V_T)V_{out} = K_4 \times (V_4 - V_T)^2 \quad (5.13)$$

$$K_3 \times (V_{in} - 2V_T)V_{out} = K_4 \times (V_{in} - V_{out} - V_T)^2 \quad (5.14)$$

Equation (5.14) cannot be easily solved. However, it can be seen that the linear operation of  $T_3$  results in a higher resistivity, leading to higher  $V_{out}$ . The validity of the assumption that  $T_3$  operates in the saturation regime will be examined in the next chapter.

The preceding analyses were based on the assumption that  $T_3$  and  $T_4$ 's  $\Delta V_T$  are the same.  $T_3$  turns on when the capacitor approaches the fully charged condition.  $T_4$  is a dynamic load, with its gate and drain connected, and is always switched on.

If the system is designed such that the circuit operates in shunt mode over a long duration,  $T_3$ 's  $\Delta V_T$  is expected to be larger than the rest of the TFTs'  $\Delta V_T$ . This is because  $T_3$  is the only TFT in the circuit which would be operating with  $V_{GS} > V_{DS}$ , leading to higher channel carrier density and therefore faster  $V_T$  shift [182]. The

assumption that transistor  $T_3$  shifts by  $V_{T3}$  and the remaining TFTs shift by  $V_T$  leads to the following modification to the  $V_{in}$ - $V_{out}$  relation:

$$\begin{aligned} K_1(V_{in} - V_{control} - V_T)^2 &= K_2(V_{control} - V_T)^2 \longrightarrow V_{control} \\ &= \frac{V_{in} - 2V_T}{\left[ \frac{\sqrt{K_2}}{\sqrt{K_1}} + 1 \right]} + V_T \end{aligned} \quad (5.15)$$

$$\begin{aligned} K_3(V_{control} - V_{T3})^2 &= K_4(V_{in} - V_{out} - V_T)^2 \longrightarrow \\ V_{out} &= \left[ 1 - \frac{1}{\alpha} \right] V_{in} - \left[ 1 - \frac{1 + \frac{V_{T3}}{V_T}}{\alpha} \right] V_T \end{aligned} \quad (5.16)$$

This is based on the assumption that  $\frac{\sqrt{K_2}}{\sqrt{K_1}} \ll 1$ . Comparing  $1 - \frac{1 + \frac{V_{T3}}{V_T}}{\alpha}$  derived above with  $1 - \frac{2}{\alpha}$  leads to the following:

$$\left( 1 - \frac{2}{\alpha} \right) - \left( 1 - \frac{1 + \frac{V_{T3}}{V_T}}{\alpha} \right) = \frac{-1 + \frac{V_{T3}}{V_T}}{\alpha} \quad (5.17)$$

If the circuit is operated under the shunt condition (e.g. a small load capacitor is used) for an extended duration of time,  $\frac{V_{T3}}{V_T} > 1$ , which leads  $\frac{-1 + \frac{V_{T3}}{V_T}}{\alpha} > 0$ . This suggests that under the shunting condition the circuit is expected to show greater instability. The validity of high  $T_3$  shift assumption is verified in the experimental stage in the following chapter.

### 5.2.3 Efficiency

The following equation relates system efficiency ( $\eta_{\text{System}}$ ) to circuit efficiency

( $\eta_{\text{Circuit}}$ ) and PV utilisation ( $\eta_{\text{PV}}$ ):

$$\eta_{\text{System}} = \eta_{\text{PV}} \times \eta_{\text{Circuit}} \quad (5.18)$$

Maximum power output is used for calculating solar cell efficiency. However, when the PV array is combined with the circuit, it does not necessarily operate at its maximum power output point. This effect is investigated by defining PV utilisation,  $\eta_{\text{PV}}$ , as following:

$$\eta_{\text{PV}} = \frac{P_{in}}{P_{Max}} = \frac{I_{in}V_{in}}{I_{sc}V_{oc}FF} \quad (5.19)$$

where  $P_{Max}$  is electrical output power at the maximum power point of the solar cell. Therefore  $\eta_{\text{PV}}$  can be 100% (when the PV cell is operating at its maximum output power point) even if the solar cell itself has an efficiency of 8%!

Using the above equation  $\eta_{\text{System}}$  can be redefined as:

$$\eta_{\text{System}} = \eta_{\text{PV}} \times \eta_{\text{Circuit}} = \frac{I_{in}V_{in}}{I_{sc}V_{oc}FF} \times \frac{I_{out}V_{out}}{I_{in}V_{in}} = \frac{I_{out}V_{out}}{I_{sc}V_{oc}FF} \quad (5.20)$$

Values of  $\eta_{\text{System}}$ ,  $\eta_{\text{PV}}$ , and  $\eta_{\text{Circuit}}$  are time dependent. It is desirable to have a high  $\eta_{\text{System}}$ , (both peak value and averaged over a charging cycle). Considering the peak value first,  $\eta_{\text{Circuit}}$  and  $\eta_{\text{PV}}$  should both reach their peak value at the same time, to achieve the maximum  $\eta_{\text{System}}$ . In the ideal charging condition,  $T_3$  is switched off (i.e.  $I_{DS_3} \ll I_{out}$ ) while the load capacitor charges. Therefore, the following approximation can be written:

$$I_{out} = I_{DS_4} \approx K_4(V_{in} - V_{out} - V_T)^2 = C_{load} \frac{dV_{out}}{dt} \quad (5.21)$$

Assuming, initially, that the load capacitor is fully discharged (i.e.  $V_{out}(t = 0) = 0$ ) and that  $V_{in}$  remains constant ( $V_{in}$  is a function of time; however it has a relatively small time derivative), the above equation can be solved to find  $V_{out}(t)$ :

$$V_{out}(t) = \frac{K_4 t (V_{in} - V_T)^2}{C_{load} + (V_{in} - V_T) K_4 t} \quad (5.22)$$

By substituting  $V_{out}(t)$  in  $I_{DS_4} \approx K_4(V_{in} - V_{out} - V_T)^2$ , the charging current,  $I_{out}(t)$ , is calculated as:

$$I_{out}(t) = \frac{C_{load}^2 K_4 (V_{in} - V_T)^2}{(C_{load} + (V_{in} - V_T) K_4 t)^2} \quad (5.23)$$

The validity of  $V_{out}(t)$  and  $I_{out}(t)$  relations can be tested in two special cases. Given that  $K_4 \ll 1$ , shortly after the start of charging, when  $C_{load} \gg (V_{in} - V_T) K_4 t$ , the following approximations can be written:

$$V_{out}(t) \approx \frac{K_4 t (V_{in} - V_T)^2}{C_{load}} \text{ and } I_{out}(t) \approx K_4 (V_{in} - V_T)^2 \quad (5.24)$$

Initially, when the capacitor is fully discharged the current through the  $T_4$  is governed by the standard saturated TFT equation,  $I_{out}(t) \approx K_4 (V_{in} - V_T)^2$ , as shown in the equation above.

The output powers can be calculated using  $I_{out}(t)$  and  $V_{out}(t)$ .

$$P_{out}(t) = I_{out}(t) \times V_{out}(t) = \frac{C_{load}^2 K_4^2 (V_{in} - V_T)^4 t}{(C_{load} + (V_{in} - V_T) K_4 t)^3} \quad (5.25)$$

The time when maximum output power is reached can be identified by solving  $\partial P_{out}(t)/\partial t = 0$ , as shown in the following equation:

$$\begin{aligned} \frac{dP_{out}(t)}{dt} &= \frac{C_{load}^2 K_4^2 (V_{in} - V_T)^4}{(C_{load} + (V_{in} - V_T) K_4 t)^3} \\ &\quad - \frac{3C_{load}^2 K_4^3 (V_{in} - V_T)^5 t}{(C_{load} + (V_{in} - V_T) K_4 t)^4} = 0 \end{aligned} \quad (5.26)$$

Solving the above equation for  $t$  and resubmitting leads to:

$$P_{out}^{max} = \frac{4K_4(V_{in} - V_T)^3}{27} \quad (5.27)$$

For this value of  $t$   $V_{out}$  and  $I_{out}$  are:

$$V_{out} = \frac{V_{in} - V_T}{3} \quad \& \quad I_{out} = \frac{4K_4(V_{in} - V_T)^2}{9} \quad (5.28)$$

The circuit should be designed so that at  $P_{out}^{max}$ ,  $\eta_{PV}$  is the highest (i.e. the PV is operated closed to the maximum power point). Typically the operating voltage at the maximum power point is defined as:

$$V_{op} = FF * V_{oc} \quad (5.29)$$

Assuming  $FF=0.7$ , the following derivation can be used to identify the optimum value for  $K_4$  to achieve the highest peak efficiency.

$$I_{out} = I_0 \left( e^{\frac{qV_{in}}{NnKT}} - 1 \right) - I_L \rightarrow V_{oc} = N \frac{nKT}{q} \ln \left( \frac{I_L}{I_0} + 1 \right) \quad (5.30)$$

$$V_{in} = 0.7V_{oc} = 0.7N \frac{nKT}{q} \ln \left( \frac{I_L}{I_0} + 1 \right) \text{ and } I_{out} = \frac{4K_4(V_{in} - V_T)^2}{9} \quad (5.31)$$

$$\rightarrow I_L + I_0 - I_0 \left( \frac{I_L}{I_0} + 1 \right)^{0.7} = \frac{4K_4 \left( 0.7N \frac{nKT}{q} \ln \left( \frac{I_L}{I_0} + 1 \right) - V_T \right)^2}{9} \quad (5.32)$$

$$\rightarrow K_4 = \frac{9 \left[ I_L + I_0 - I_0 \left( \frac{I_L}{I_0} + 1 \right)^{0.7} \right]}{4 \left[ \left( 0.7N \frac{nKT}{q} \ln \left( \frac{I_L}{I_0} + 1 \right) \right) - V_T \right]^2} \quad (5.33)$$

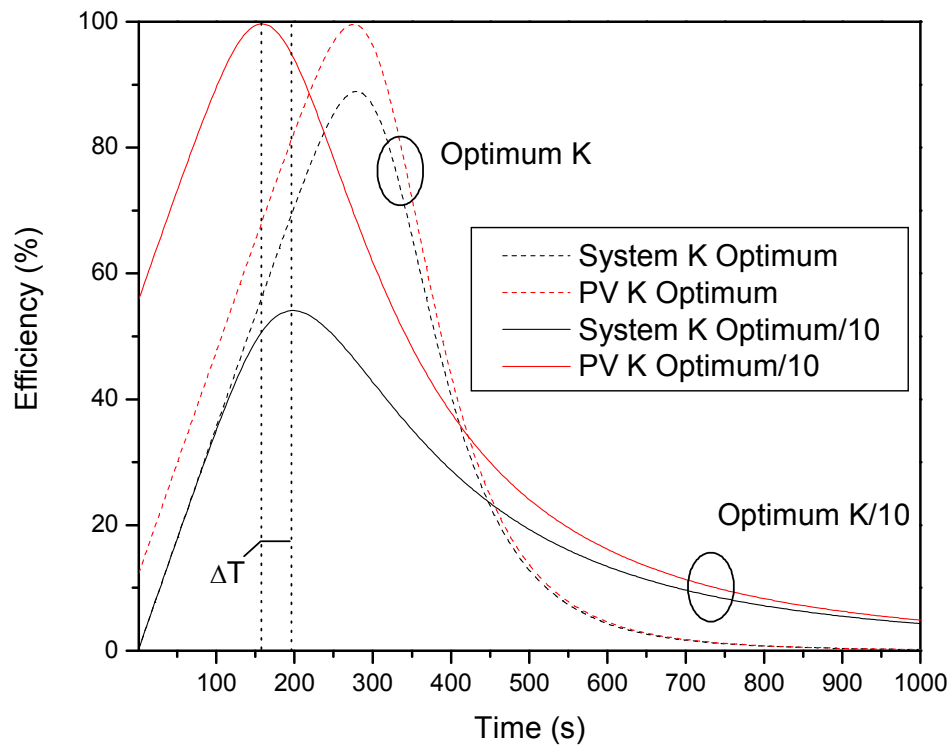
A simple SPICE model consisting of a PV array, gate-drain connected FET (T<sub>4</sub>), and capacitive load was implemented. In line with the approximations made, T<sub>3</sub> is neglected in this simulation. The Table 5-2 shows some of the values used in this model.

	<i>Typical Range</i>	<i>Value used</i>	<i>Value used</i>
$K_4$	$10^{-5} \sim 10^{-4}$ per TFT	0.0013	0.00013
$I_0$	$1 \sim 10$ pA/cm <sup>2</sup>	$10^{-15}$	$10^{-15}$
$I_L$	$0.1 \sim 10$ mA/cm <sup>2</sup>	$10^{-7}$	$10^{-8}$
$V_T$	0~5V	1	1
$V_{oc}$	5~50	20	20

**Table 5-2 Typical PV array values and corresponding optimum  $K_4$**

As Figure 5-4 shows, when  $K_4$  is smaller than its optimum value, there is a time lag between the peak  $\eta_{PV}$  and  $\eta_{System}$  suggesting a time lag between the peak  $\eta_{Circuit}$  and  $\eta_{PV}$ .

One important factor is the relation between the  $\eta_{\text{System}}$  efficiency and value of  $K_4$ . This is shown in Figure 5-5. It can be seen that approximately when  $\frac{K_4}{\text{Optimum } K_4} > 1$ , peak system  $\eta_{\text{System}}$  starts to saturate, and for values below this peak  $\eta_{\text{System}}$  drops sharply. The drop is more significant for larger short circuit currents (and therefore light intensity).



**Figure 5-4 Variation in system efficiency and PV array efficiency with time for an optimised and non-optimised system**

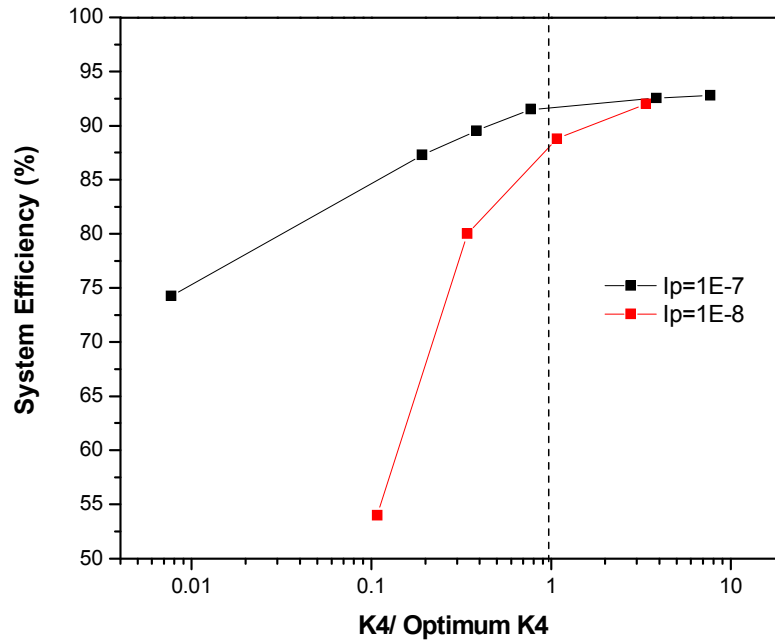
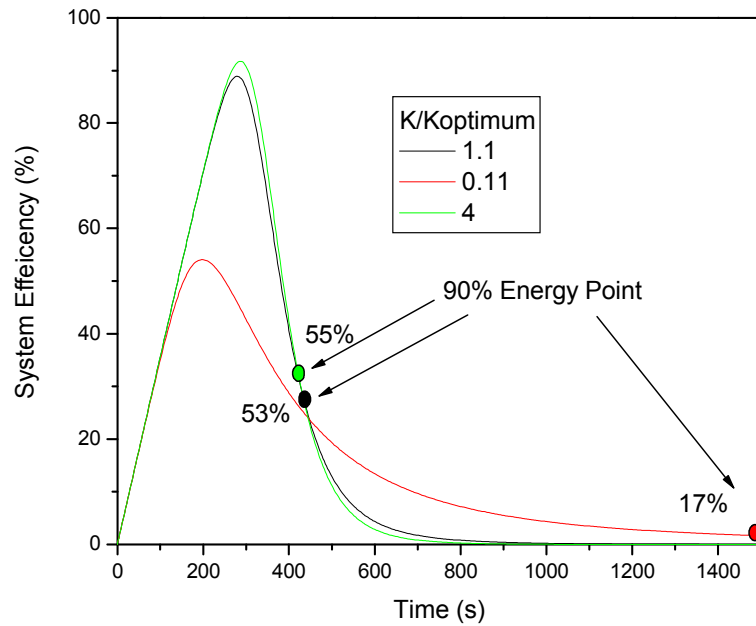


Figure 5-5 Effect of  $K_4$  on peak system efficiency at two different light intensities

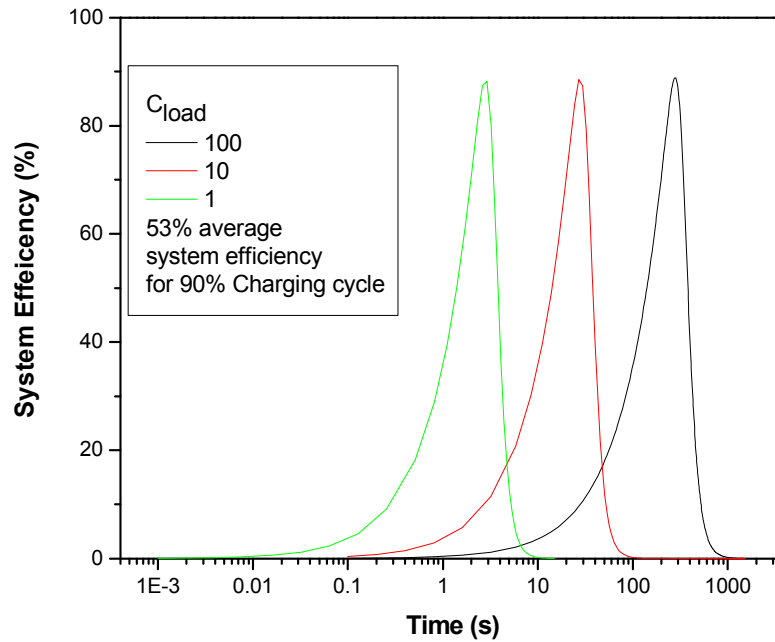
As well as peak efficiency, average system efficiency is also an important parameter to consider. Figure 5-6 shows that the system efficiency of a non-optimised  $K_4$  becomes higher than that of an optimised  $K_4$  at longer times. However this does not mean that a non-optimised  $K_4$  has a higher average efficiency. Efficiency of optimised  $K_4$  approaches zero because the capacitor is fully charged. One way of comparing average efficiency is to consider the energy used to charge the load capacitor to 90% of its capacity. Figure 5-6 shows the average efficiency when  $\frac{K_4}{\text{Optimum } K_4} > 1$ , is over 50%, with a sharp drop for  $\frac{K_4}{\text{Optimum } K_4} < 1$ .





**Figure 5-6 Effect of  $K_4$  optimisation on average efficiency**

The optimisation equation developed earlier suggests that the  $K_4$  value is independent of the load capacitor, suggesting that peak and average efficiency values are independent of the load capacitance. Figure 5-7 shows the simulation results for different load capacitances. As expected different capacitor values store different amounts of energy, resulting in a change in the time needed to reach peak efficiency. However its value remains constant. Furthermore, the average efficiency for a 90% charge cycle remains constant. This suggests that when selecting the capacitor size, the main consideration should be the amount of energy needed to be stored.



**Figure 5-7 Effect of load capacitance on the system efficiency**

The optimisation equation suggests a link between the PV array's  $V_{oc}$  and the minimum value of optimum  $K_4$  and thus the size of the array. This is shown in Figure 5-8. However, this figure is incorrect as it does not take into account the  $T_3$  operation. As the array size is increased,  $T_3$  becomes leaky earlier, resulting in the shunting of electrical power and loss of efficiency.

Figure 5-9 shows the general trend for the minimum value of  $K_4$  needed as a function of  $I_{sc}$  and thus light intensity. It can be seen that the dependence is linear over a wide range of values. However, it should be noted that the value of FF is dependent on the  $I_{sc}$ , resulting in a deviation from Figure 5-9.

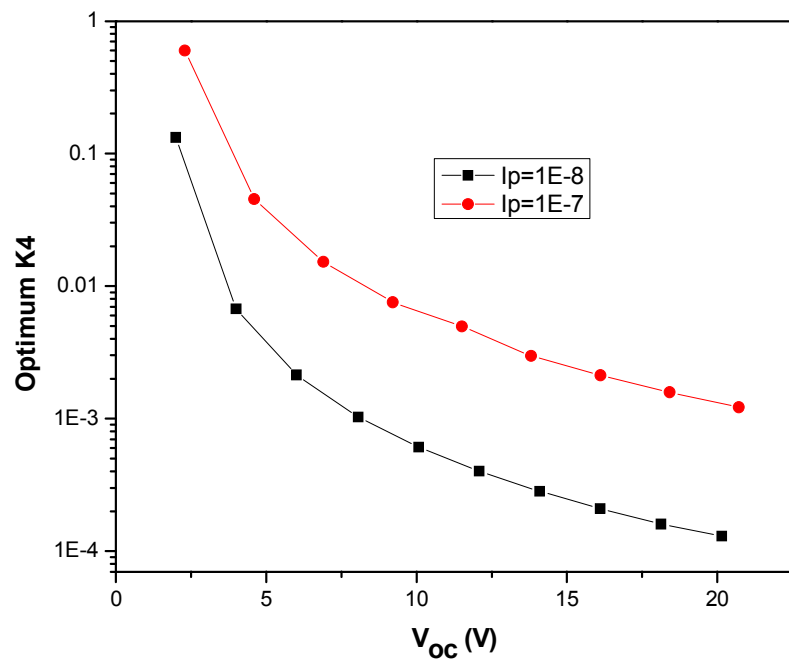


Figure 5-8 Incorrect effect of PV array's size on the optimum  $K_4$

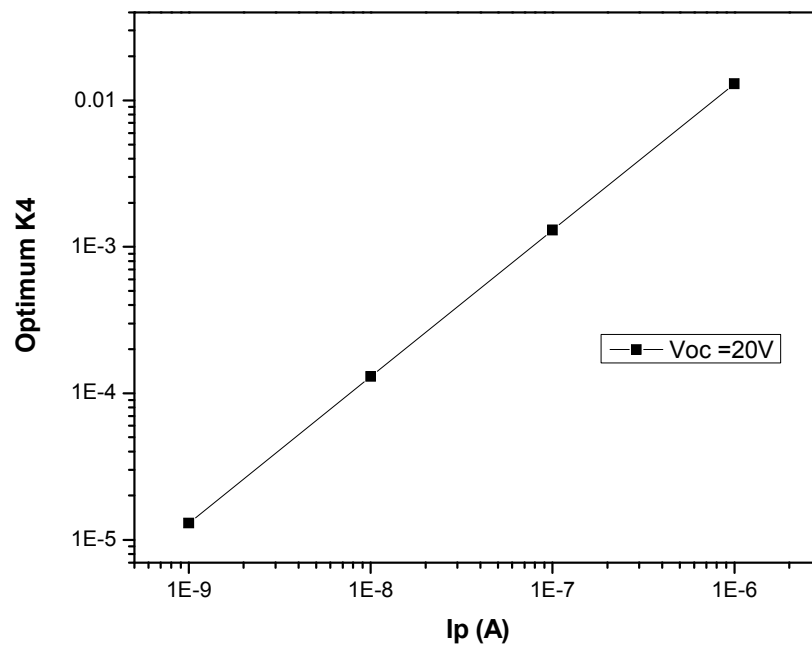
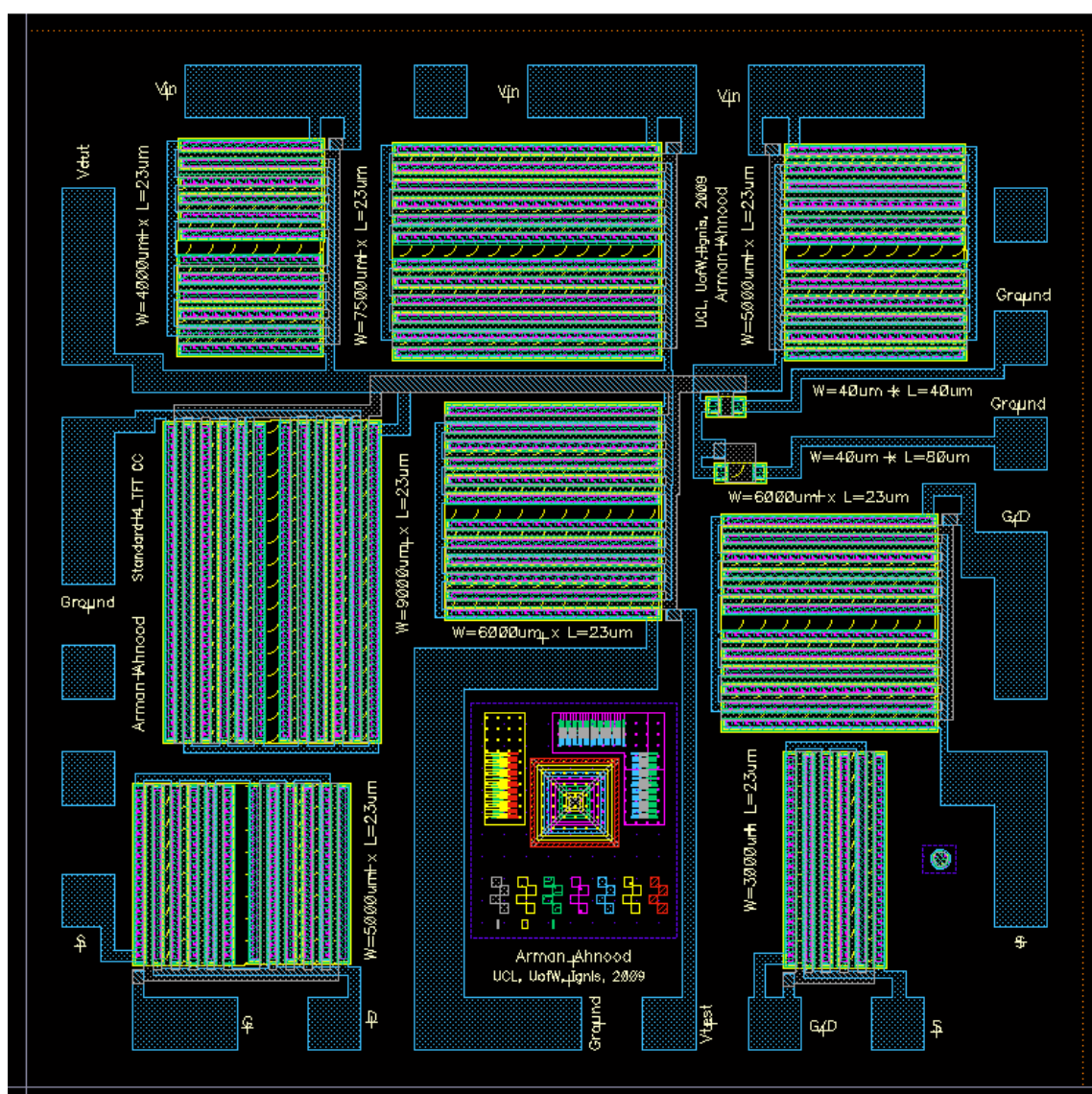


Figure 5-9 Effect of  $I_{sc}$  on the optimum value of  $K_4$

The circuit was designed for this work using Cadence layout design software. The general layout of the circuit is shown in Figure 5-10. TFT design rules developed at the University of Waterloo were followed in this work. Few redundancies were included in the circuit. Table 5-3 shows TFTs' width/length ratios. To achieve the large values of W/L, the TFT layout was designed as a series of "interdigitated fingers".



**Figure 5-10 Circuit layout design used in this work**

<i>TFT</i>	<i>T1</i>	<i>T2</i>	<i>T3</i>	<i>T4</i>
<b><i>W/L (μm)</i></b>	5000/23	40/80	6000/23	7500/23

Table 5-3 Channel width/length ratios of TFTs used in the circuit

The following equation can be written for a TFT operated in saturation:

$$I_{DS} \approx K(V_{GS} - V_T)^2 = \frac{W}{2L} \mu_{FE} C_{SiN} (V_{GS} - V_T)^2 \quad (5.34)$$

Therefore, assuming the same dielectric capacitance ( $C_{SiN}$ ) and field effect mobility, the ratios of TFT transconductances are proportional to the channel widths. This results in a  $K_2/K_1$  value of close to 0.002, in line with the requirements outlined in the previous section. The ratio of  $K_4/K_3$  is 1.25, leading to  $\alpha=1.12$ . Using this value of  $\alpha$ , the following can be written:

$$V_{out} = \left[1 - \frac{1}{\alpha}\right] V_{in} - \left[1 - \frac{2}{\alpha}\right] V_T = 0.11V_{in} + 0.77V_T \quad (5.35)$$

$$\text{when } V_{in} < (2 + \alpha) \times V_T = 3.12 \times V_T$$

Based on the above equation and using  $V_T = 1.8$  extracted in section 3.4.2, the maximum voltage required to achieve saturation in the circuit is 5.6V.

Using a W/L ratio of 7500/23 for  $T_4$ , with a device mobility of  $1\text{cm}^2/\text{V.s}$  and 300nm SiN:H, leads to  $K_4$  of approximately  $3 \mu\text{s}$ . Comparing this value to the values shown in Figure 5-9, suggest that the circuit would be capable of handling only small values of  $I_{sc}$  without significant degradation of efficiency.<sup>10</sup>

<sup>10</sup> The circuit was initially designed based on higher mobility assumptions.

A number of assumptions are made in these calculations. The saturation equation is a crude approximation. Furthermore, contact resistance is neglected in here, and is likely to play a significant role for the short channels used in this work.

## 5.4 Solar Cell Array Design

Individual cells are connected in series to form an array with useful output voltage and current. Figure 5-11 shows the cross sectional diagram of the cell interconnections which will be used in the project.

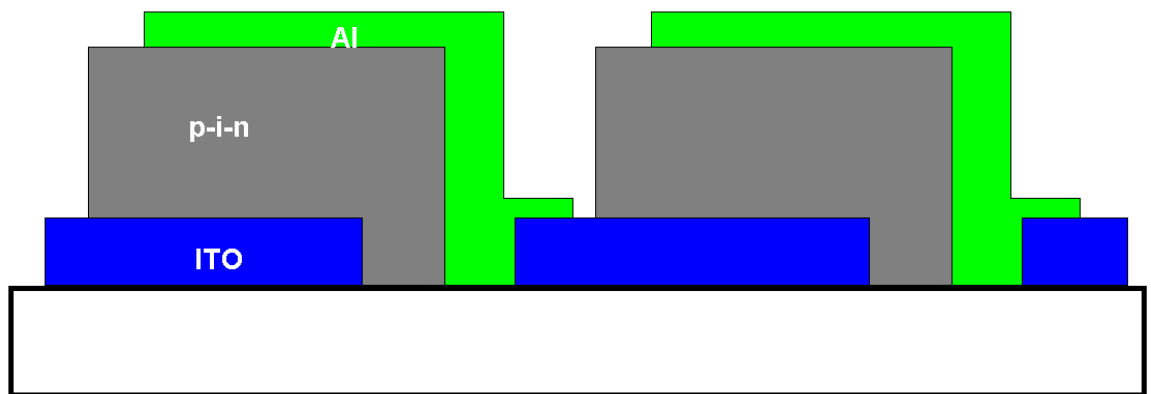
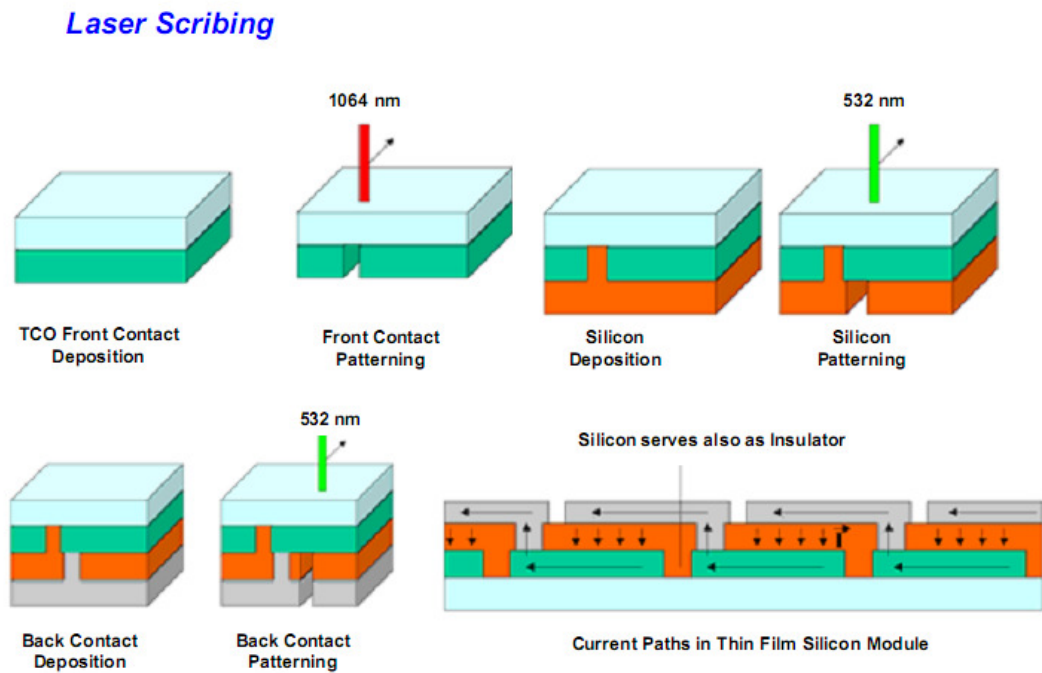


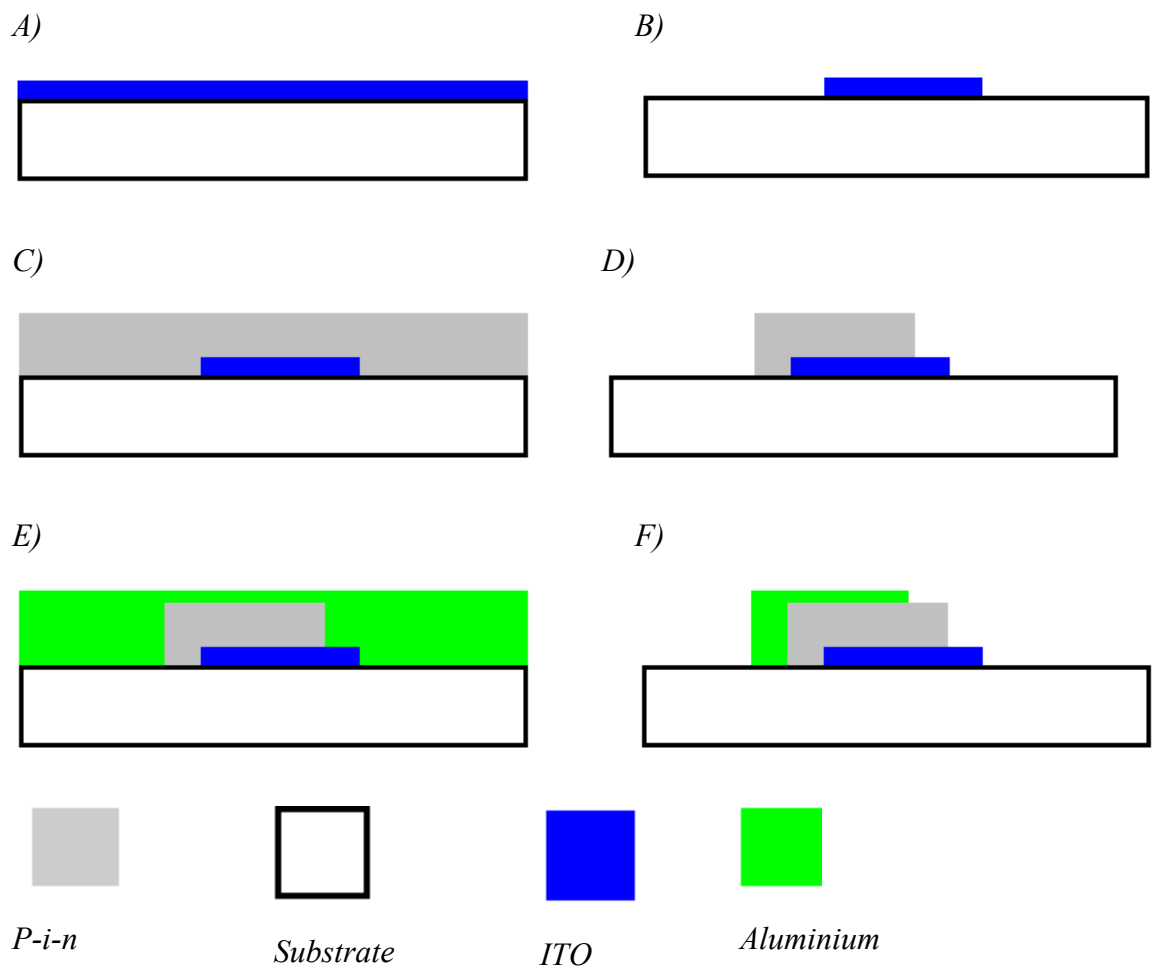
Figure 5-11 Cross sectional view of solar cell interconnection

In conventional PV array fabrication laser scribing is used to pattern the contact electrodes and silicon layers. Figure 5-12 outlines the basic steps of a typical PV array fabrication process.



**Figure 5-12** Flow diagram of conventional PV array fabrication process. Taken from [5]

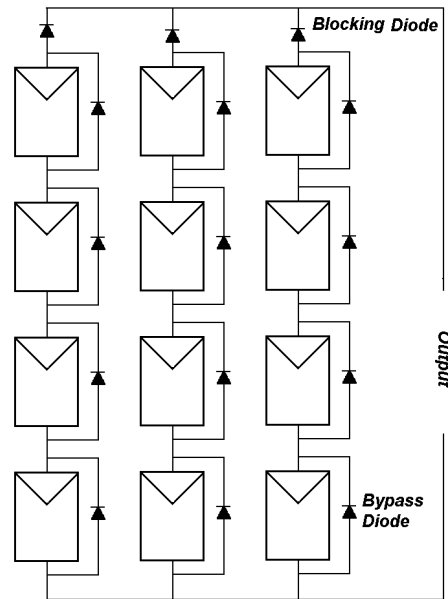
Photolithography, rather than laser scribing will be used to pattern the features to ensure compatibility with plastic substrates. Due to the small scale of this project, standard photolithography tools can be used. Figure 5-13 shows the process steps used for the fabrication of the PV array in this work. Etching of the ITO was done using HCl/H<sub>2</sub>O (1:1) at room temperature. The dry etch process (pressure of 70mBar, power 100W, SF<sub>6</sub> flow rate of 50sccm, duration of 15min) was used for etching the silicon films. The aluminium was etched using wet aluminium etchant.



**Figure 5-13 PV array process flow diagram**

Figure 5-14 shows an array of interconnected solar cells. This array shows three lines of serially connected devices. Each serial connection consists of 4 connected cells. The solar cells should be designed such that the current through each of the cells, and the voltage at each line is equal. Despite the design, variation in the fabrication and non-uniform light intensity will result in a variation in the operating current and voltages between the cells.





**Figure 5-14** An array of connected cells with bypass and blocking diodes adopted from [183]

Variation in operating current of serially connected cells results in the dissipation of power in the cell, formation of hot spots, and possible damage to the cell with the hotspots. A bypass diode can be used to provide an alternative conduction path, bypassing the cell with low current. However, due to the scale of this work, the current in the cell will be small. Therefore the power dissipation in the cell will be small and will not result in hotspot damage, thus a bypass diode will not be used [184].

Differences in operating voltages of the parallel lines may result in the dissipation of power in one of the lines. Blocking diodes can be used to avoid this problem. However, a blocking diode will reduce the output power of each line, due to the voltage drop across it. Furthermore, given that the combined breakdown voltage of each serial line is likely to be higher than the output voltage of the line, the blocking diode will be unnecessary and is omitted in this work [184].

Figure 5-15 shows the layout of a PV array used in this work. Two types of PV arrays with different area cells were designed:  $100\mu m \times 100\mu m$  and  $200\mu m \times 200\mu m$ . Outputs were taken such that 8, 16 and 24 cells in series could be tested.

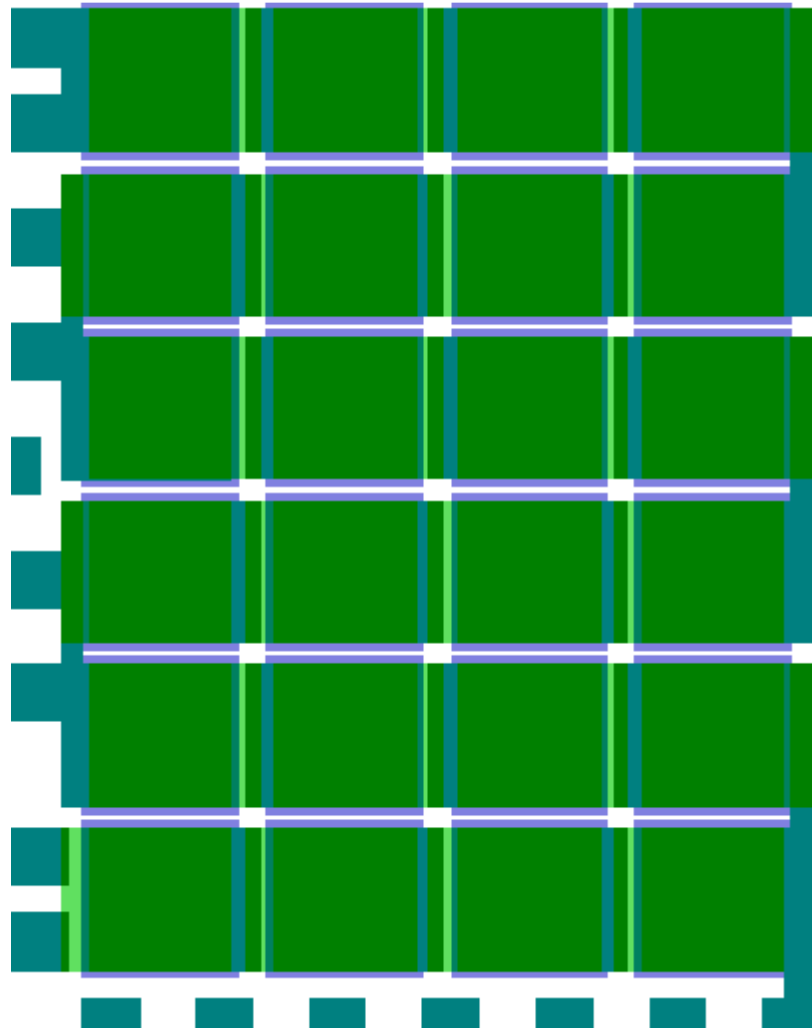


Figure 5-15 PV array layout design

## 5.5 Summary and Conclusions

In this section one possible circuit design for regulating the PV array is proposed. Using approximate TFT equations, the circuit behaviour is analysed. It was shown that depending on the TFT geometries, it is possible to compromise between long term

stability of output voltage, and the stability of the output voltage under various light intensities.

The system efficiency was related to circuit efficiency and PV utilisation. The relation between the dynamic load TFTs' transconductance and system efficiency was explored, and possible methods of optimising system efficiency proposed.

The circuit and PV array designs are presented and discussed. The PV array fabrication process is described and compared with the standard PV array fabrication process.

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## 6 System Results

### 6.1 Solar Cell

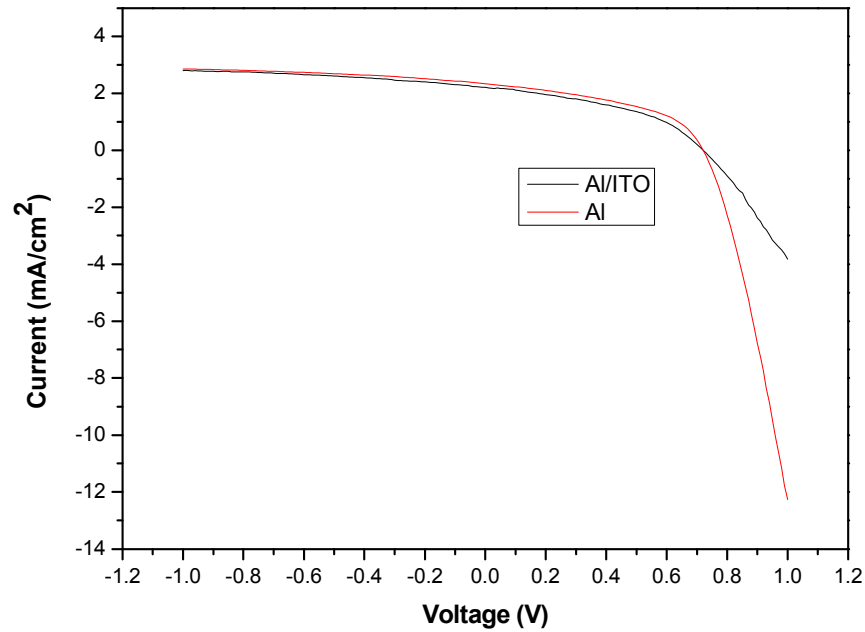
#### 6.1.1 Discrete PV Device

Photovoltaic devices were fabricated using the steps outlined in section 5.4. Given the small size of contacts, the photovoltaic devices were measured in a probe-station, using probe-arms. A microscope light (halogen lamp), was used for the illumination. Light was coupled to the device using a mirror placed at  $45^\circ$  to the plane of the substrate. In this section results on discrete PV device are presented.

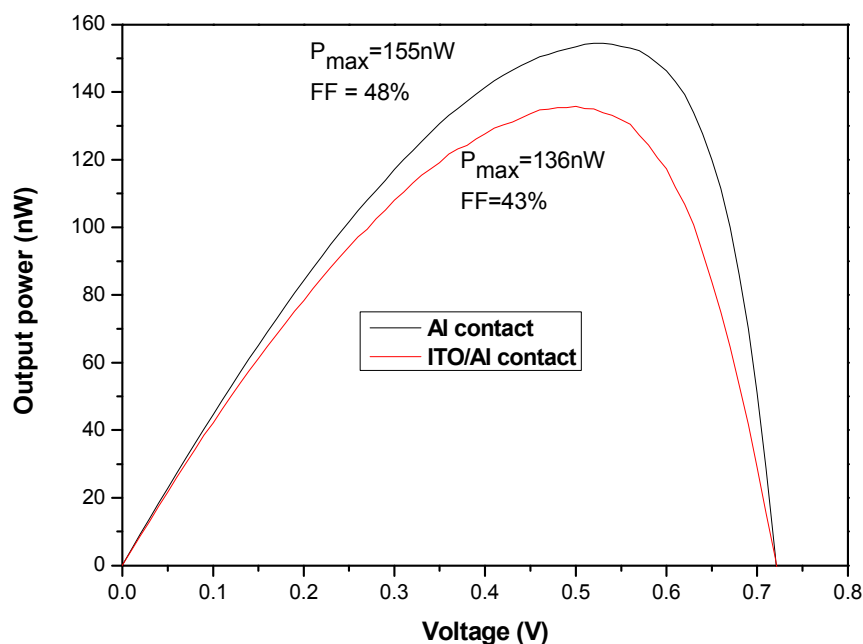
Under illumination the device exhibited a significant drop in the fill factor. One possible reason for degradation in the fill factor is high series resistance. Junction resistance at the ITO/Al interface, and poor sidewall coverage of evaporated Al can be two possible reasons for high series resistance. In order to investigate the significance of these effects, the PV cell was probed at the ITO contact and at the Al contact (directly above the p-i-n). The first measurement includes effects of both ITO/Al junctions and sidewall coverage. The second probing location excludes the two effects.

Figure 6-1 and Figure 6-2 show the effect of probing location on characteristics of an illuminated PV device. Figure 6-1 shows a significant difference between ITO probing and Al probing in the forward direction (high current density). As shown in Figure 6-2,

measurement at the Al contact results in an increase in the fill factor compared to ITO probing. This is consistent with the series resistance hypothesis and can be due to the poor contact at the Al/ITO junction [185]. However the fill factor is still significantly less than the values obtained for the standard PV described in section 4.2.3.

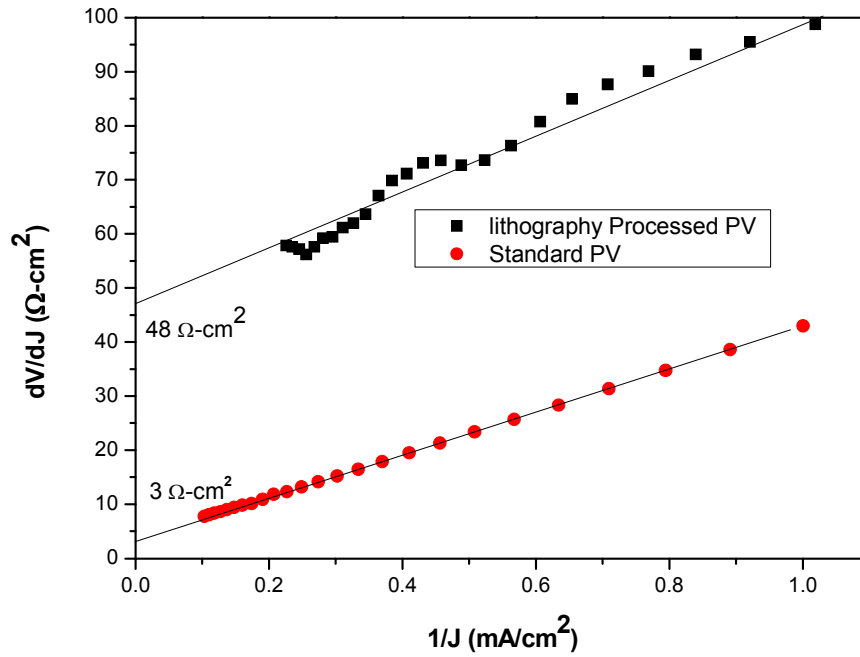


**Figure 6-1 Photocurrent-voltage characteristics of a single p-i-n PV cell – low, non-standard light source**



**Figure 6-2 Power-voltage characteristics of a single p-i-n PV cell – low, non-standard light source**

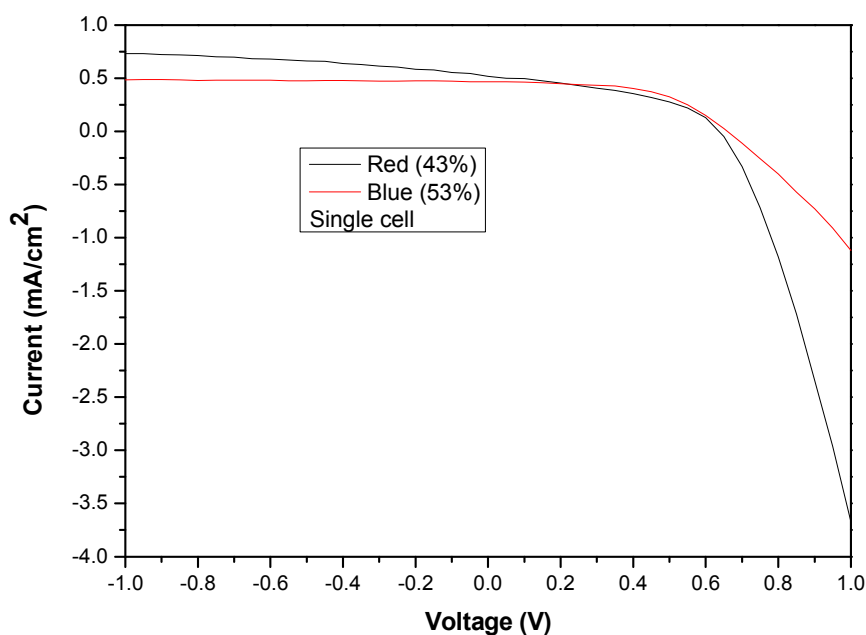
Another reason for high series resistance is the process related defects created during the fabrication stage between the n-type nc-Si:H and evaporated Al. This is investigated by extracting series resistance from dark current-voltage characteristics of a photolithographically (PL) processed PV cell and a standard PV cell using the same process conditions. For the extraction of series resistance the method outlined by SS Hegedus (1997) is used [186]. The results are shown in Figure 6-3. The graph shows over one order of the magnitude increase in the series resistance of the PL processed cell compared with the standard one. This suggests that process related defects result in the degradation of the device, contributing to a reduction in the fill factor.



**Figure 6-3 Series resistance for standard and processed PV using the same deposition condition**

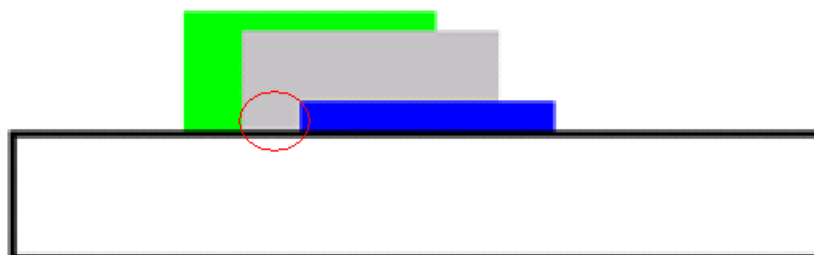
Fill factor can also be affected by the collection efficiency of the photocarriers. Such an effect results in a wavelength dependent fill factor, depending on the penetration depth and the carrier loss mechanism. Figure 6-4 shows the current-voltage characteristics of a PV device illuminated with blue (450nm) and red (650nm) light. This approach is used to look at the losses in the p-i interface and i-layer respectively. The intensity of light was adjusted to achieve similar short circuit current. It can be seen that the fill factor drops from 53% to 43% when switching from blue to red illumination. This suggests some loss mechanism in the intrinsic layer. However, the value of the fill factor does not revert to the original value obtained for the conventional cell as shown in Figure 4-16, pointing to additional loss mechanisms.





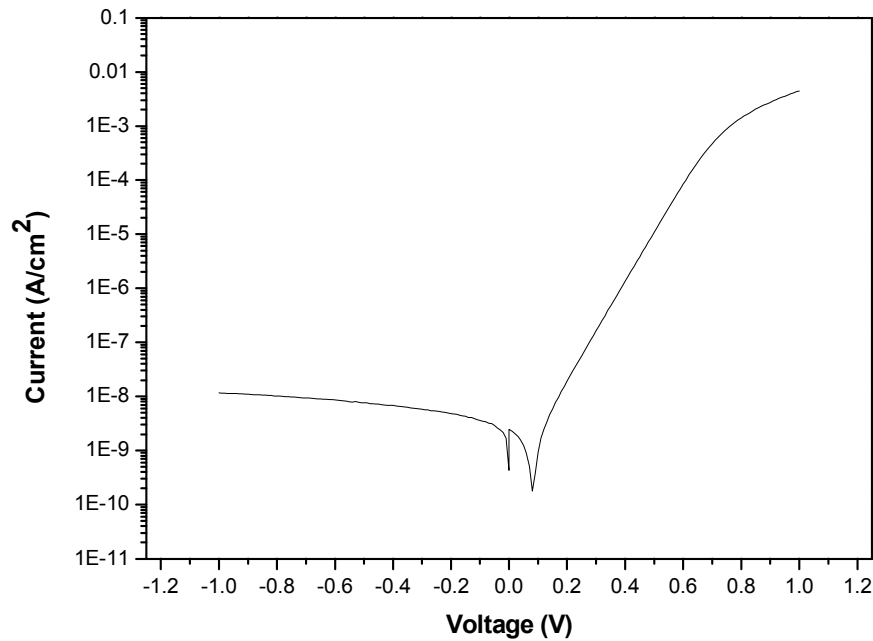
**Figure 6-4 I-V characteristics of a single PV device under blue and red illumination**

Fill factor can also be affected by the shunt resistance. There are a number of pathways for the shunt resistance. For example, leakage between the aluminium and ITO (highlighted by the red circuit in Figure 6-5), shunting of the i-layer by aluminium on the sidewall, or shunting due to the sidewall IRE defects. The effect of such defects can also be wavelength dependent (due to the penetration depth). They can be partly minimised by increasing the spacing of the aluminium and ITO (set at 50  $\mu\text{m}$  in this work).



**Figure 6-5 Possible shunting pathway between ITO and aluminium**

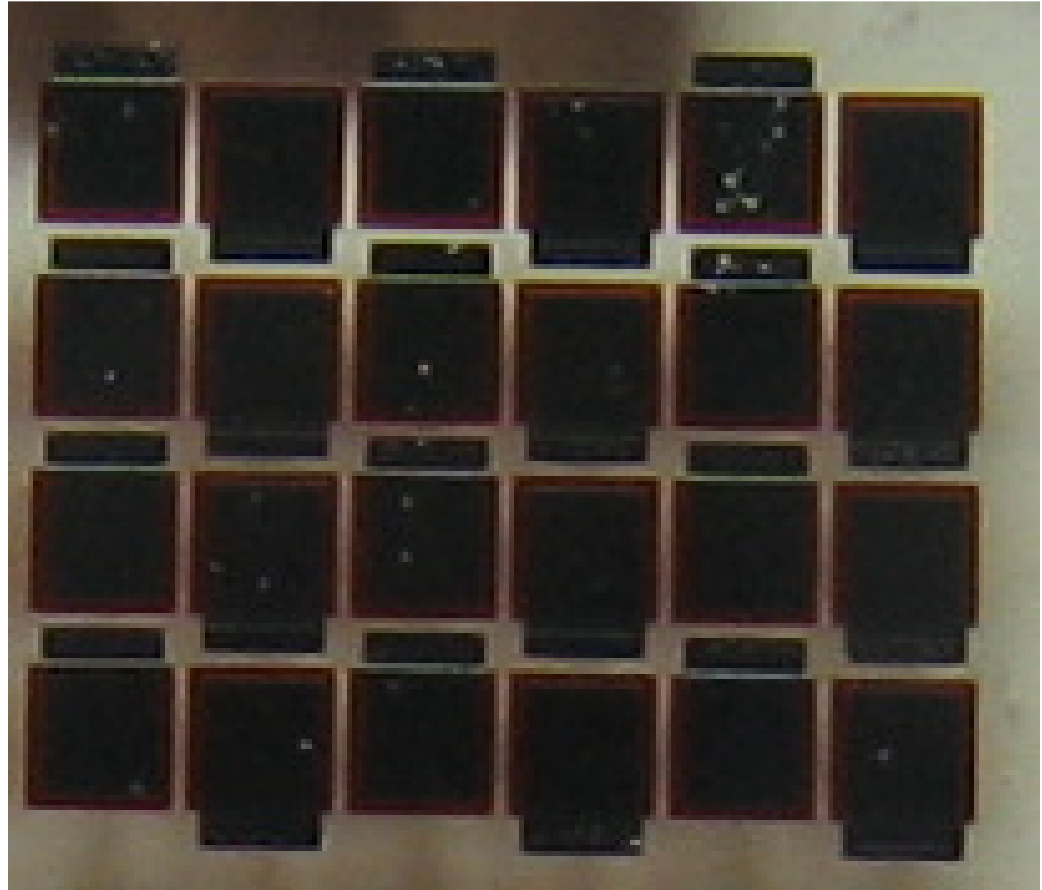
The dark I-V characteristics' tool is useful for probing PV devices. Figure 6-6 shows the dark I-V of a single device from which a reverse saturation current density of 314 pA/cm<sup>2</sup> and diode ideality factor of 1.87 can be extracted. Both of the values are higher than the values reported for a standard p-i-n diode ( $J_0=5.02$  pA/cm<sup>2</sup> and  $n = 1.56$ ). This is consistent with the poor performance of the PL processed PV device compared to the standard processed PV device presented in chapter 4.



**Figure 6-6** Dark current-voltage characteristics of the processed PV device (100μm x 100μm cell)

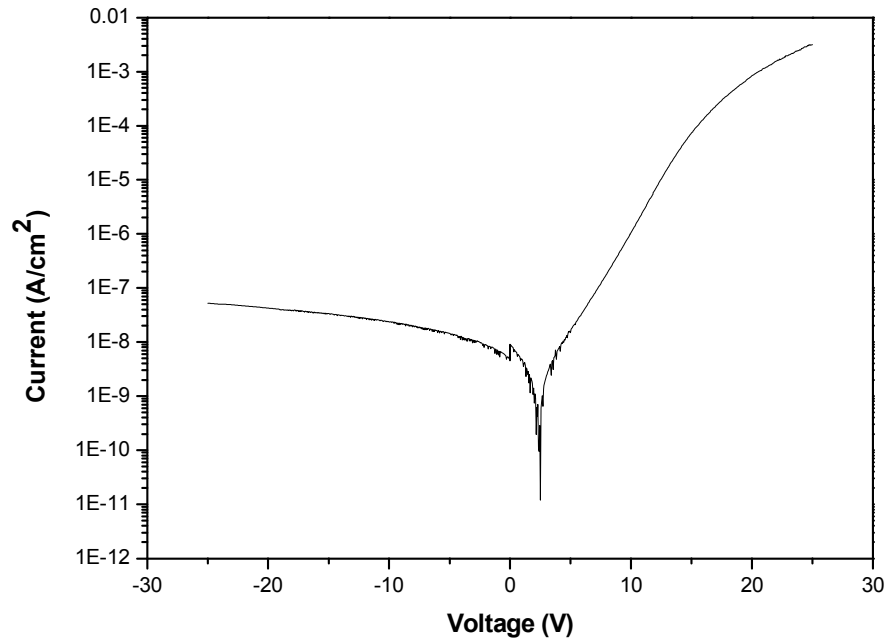
### 6.1.2 PV Array

A 24 cell array was measured using the same method outlined for a single PV cell. Figure 6-7 shows the p-i-n array (each cell 100μm×100μm) fabricated for this work. The cells are connected to each other using Al and ITO. The ITO contact layer is not visible in this photograph.



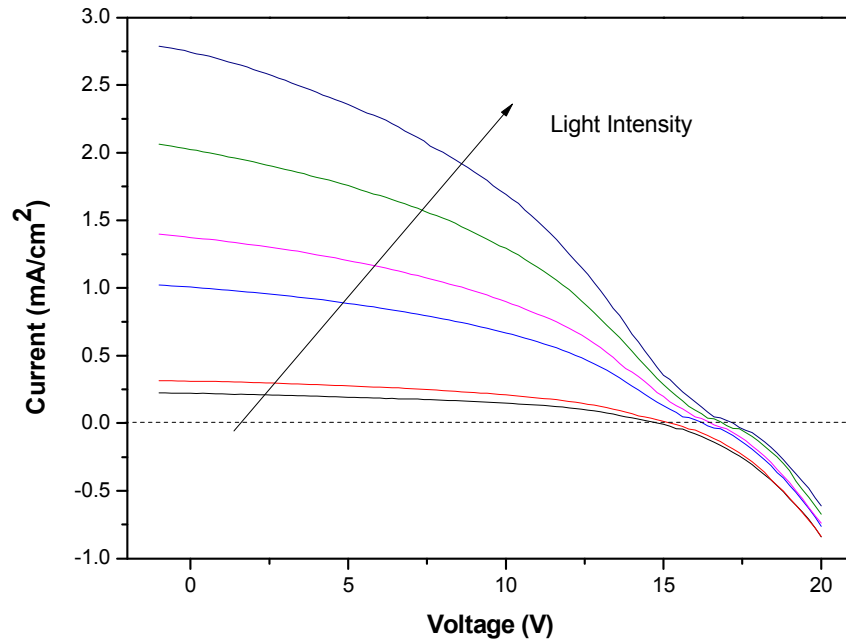
**Figure 6-7 Photograph of p-i-n array fabricated in this work**

The dark current-voltage characteristic of an array was measured, the result of which is shown in Figure 6-8. The diode characteristics were extracted between 5V and 14V, yielding a slope overall factor of 44.16 (corresponding to a diode quality factor of 1.84), consistent with the results obtained from a standard PV cell extracted in chapter 4. However, the quality factor differs for the lithographically processed cell reported in 6.1.1. This difference can be due to parasitic resistances, which are significant for this sample.



**Figure 6-8 Dark I-V characteristics of 24 cell array.**

Figure 6-9 shows the effect of light intensity of the I-V characteristics of the p-i-n array. An increase in the light intensity results in an increase in the  $V_{oc}$  and  $I_{sc}$  and a reduction of fill factor which is consistent with standard PV devices. However, Figure 6-9 shows a double-slope behaviour, close to  $V_{oc}$ . This becomes increasingly dominant as the light intensity is increased. This type of behaviour was not observed in either the discrete lithographically processed PV test structures or the conventional PV devices in the measurement range used. To rule out any transient effects, the measurement was performed with different time settings, which yielded the same results. The origin of this behaviour is not clear, and detailed investigations are needed to identify it. However this was not done in this work.



**Figure 6-9 Effect of light intensity on current-voltage characteristics of 24 cell p-i-n PV array – non-standard light source**

As outlined in section 4.2.3 the relation between the  $J_{oc}$  and  $V_{oc}$  for a single cell follows the equation below:

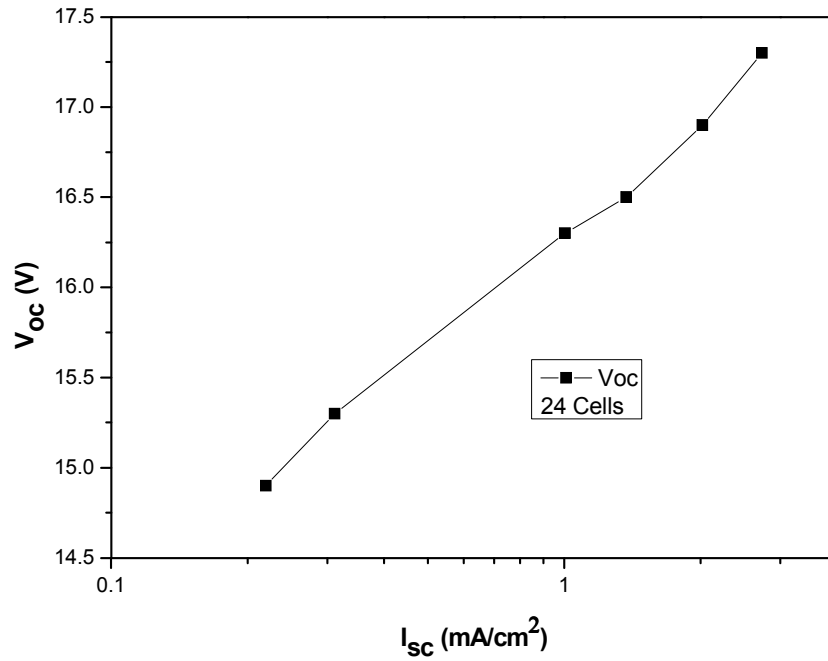
$$J_{sc} = J_0 \text{Exp} \left( \frac{qV_{oc}}{nKT} \right) \quad (6.1)$$

For an array this can be modified to the following:

$$J_{sc} = J_0 \text{Exp} \left( \frac{qV_{oc}}{NnKT} \right) \quad (6.2)$$

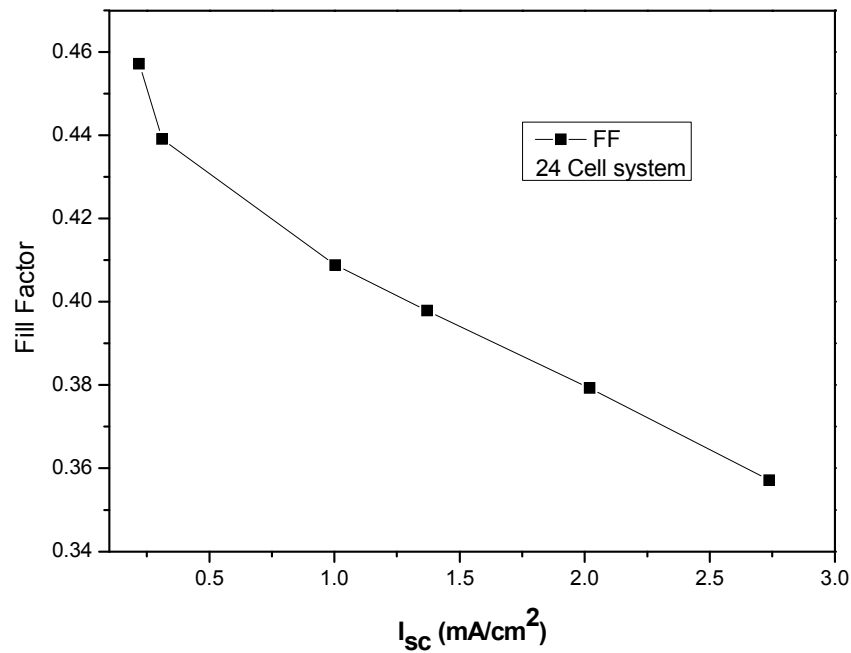
where  $N$  is the number of cells and  $n$  is the quality factor. Figure 6-10 shows the relation between the  $J_{oc}$  and  $V_{oc}$ . The curve does not appear to yield a straight line, due to non-idealities in the device, outlined earlier. From this graph the slope of  $0.907 \pm 0.03$

is extracted which results in the diode quality factor of  $1.78 \pm 0.06$ . This value is within the range of values extracted from the dark I-V characteristics although it appears to be slightly lower.



**Figure 6-10 Short circuit current vs. open circuit voltage for 24 cell array**

The value of FF depends on short circuit current and light intensity. This is due to a combination of shunting, series resistance and the p-i-n quality. Figure 6-11 shows the variation in the array fill factor with light intensity. A continuous drop in the fill factor can be observed with increasing light intensity. This behaviour has been attributed to the presence of significant series resistance [187] [188].



**Figure 6-11 Fill factor vs. short circuit current for 24 cell array**

In addition to light intensity the number of cells within an array affects the array's  $V_{oc}$  and FF. Figure 6-12 and Figure 6-13 show the effect of array size on  $V_{oc}$  and FF. Under illumination which results in a short circuit current of  $1\text{mA/cm}^2$ , open circuit voltage varies linearly with the cell numbers. 0.72V per cell can be extracted from Figure 6-12. The FF drops as the number of cells is reduced. A similar trend has been observed and reported for a standard PV array [188].

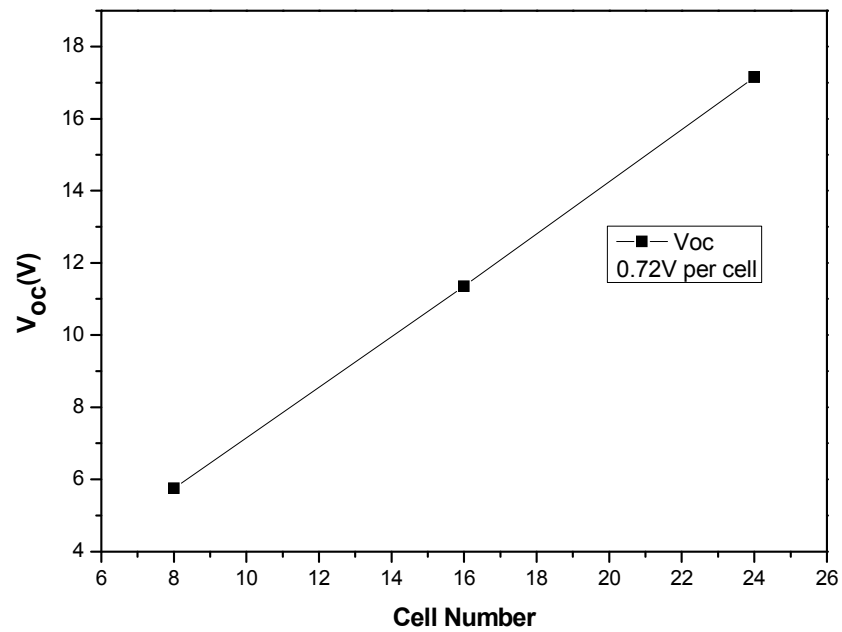


Figure 6-12 Effect of PV array size on the open circuit voltage

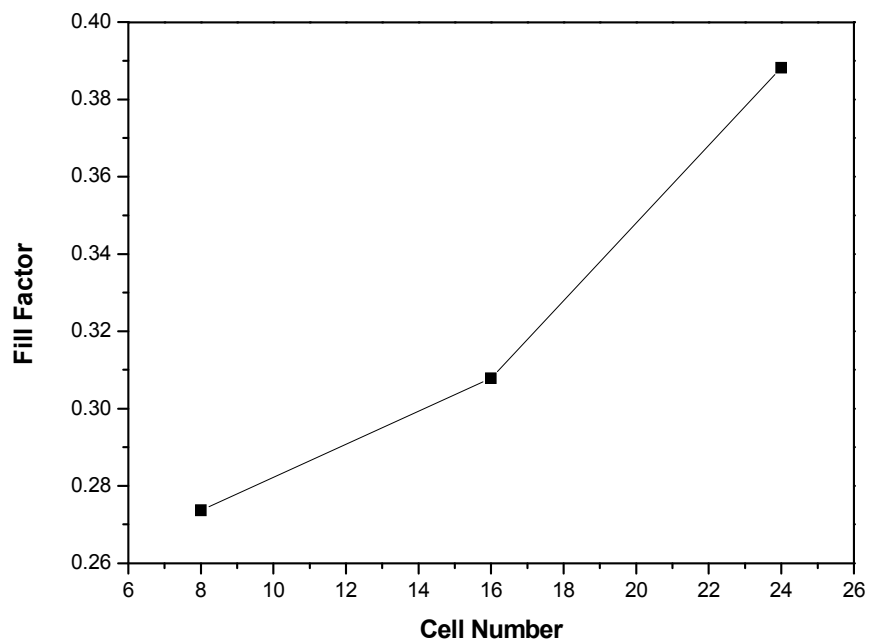


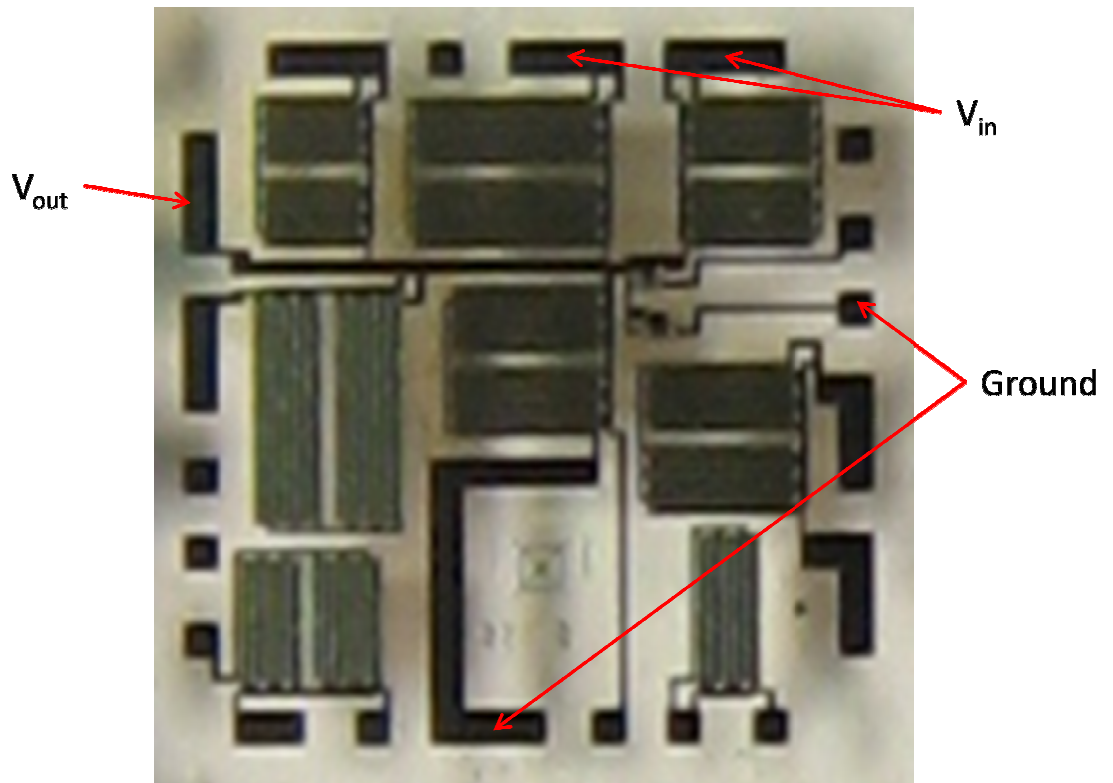
Figure 6-13 Effect of PV array size on the fill factor



## 6.2 Circuit Measurement

### 6.2.1 Measurement Set-up

Figure 6-14 shows the fabricated circuit. Various input-output connections are labelled in the diagram.



**Figure 6-14 Photograph of the fabricated circuit. Labels show the connections.**

Figure 6-15 shows the schematic diagram of the experimental set-up used to test the system. The TFT circuit is sensitive to light due to the photo-absorption in the channel. For applications where the TFT is expected to be exposed to light (e.g. used in displays) an additional metallic light-shield layer is used to avoid any photo-response. Given the preliminary nature of this work, this layer was omitted from fabrication. Therefore the circuit was set up in a low noise probe station which would also act as a light-shield. The PV array was set up in a second probe station, along with a light source (halogen

lamp). Probe arms were used to connect it to the PV array. A combination of co-axial and tri-axial cables was used to connect the PV array to the circuit. The series resistance of the cables was neglected. The output of the circuit was connected to electrolytic capacitors with various values ( $1\mu\text{F}$ ,  $10\mu\text{F}$ ,  $100\mu\text{F}$ ). The size of load capacitance was changed depending on the light intensity to achieve an appropriate charging time (a few 100s).

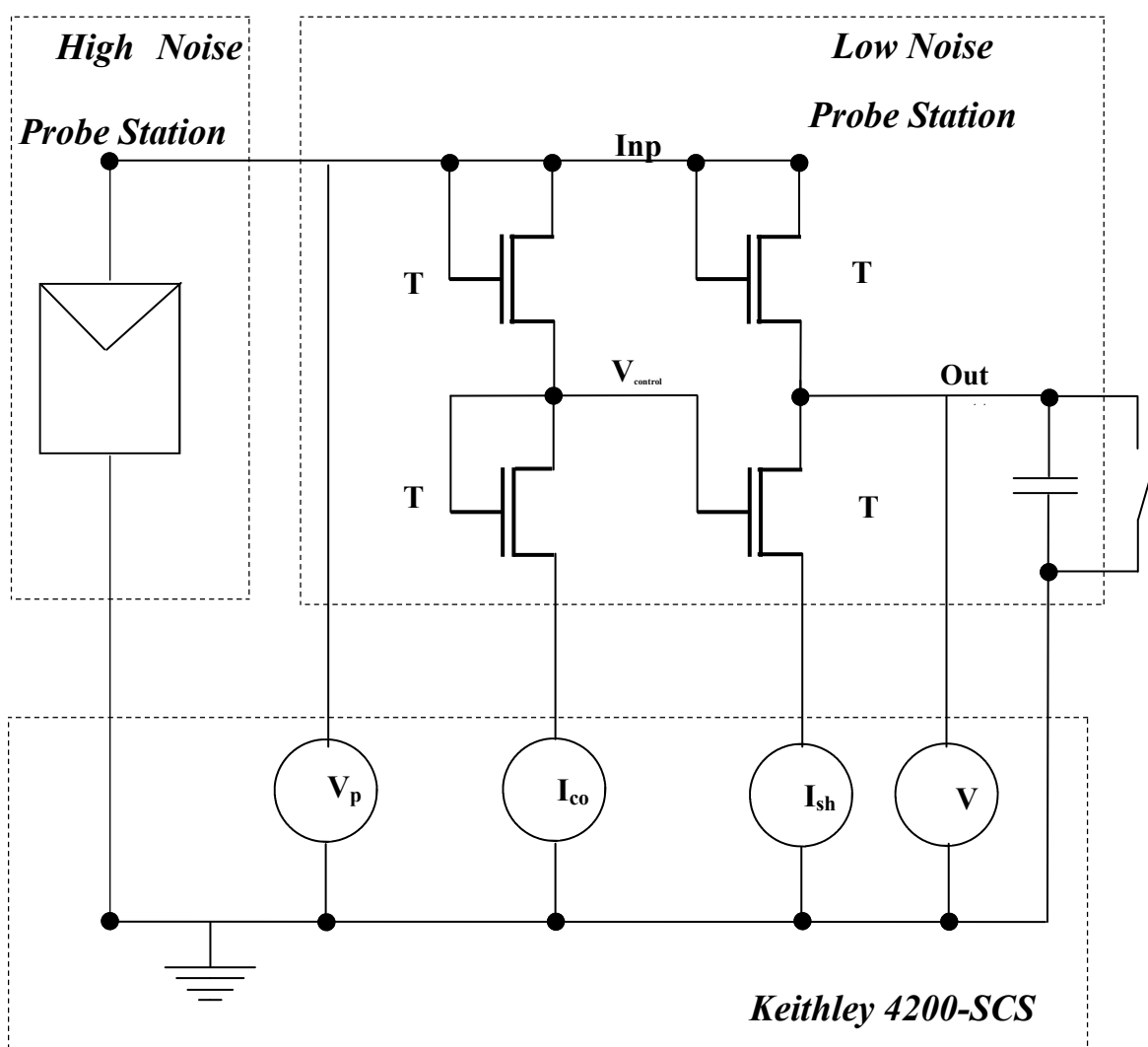


Figure 6-15 Schematic of experimental set-up used for testing of the circuit

The Keithley 4200 semiconductor characterisation system (4200-SCS) was used to provide a low noise common ground. The 4200-SCS had 4 source measurement units (SMUs) with pre-amplifiers which were used to measure the current through the shunt path ( $I_{\text{shunt}}$ ) and the control path ( $I_{\text{control}}$ ) as well as the input voltage ( $V_{\text{pv}}$ ) and output voltage ( $V_{\text{out}}$ ). The output current was calculated using the following equation:

$$\text{---} \quad (6.3)$$

Input current was calculated using the following equation:

$$(6.3)$$

A range of light intensities and load capacitances was tested in this work. Each time light intensity was changed photo I-V characteristics of the array were measured by reconfiguring the connections and using the 4200-SCS.

Comparisons for the circuit response under various light intensities were simplified by “normalising time”:  $t \times C / I_{\text{in}}$ . Using the experimental set-up described, a number of measurements were performed. They can be grouped into 3 categories as shown in Figure 6-16:

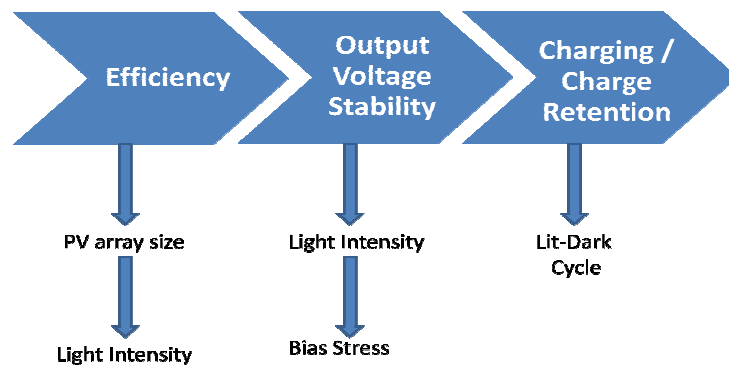


Figure 6-16 Measurement approach

### 6.2.2 System Efficiency

Figure 6-17 shows the effect of the PV array size on the peak system efficiency, under a fixed light intensity. System efficiency is defined as:

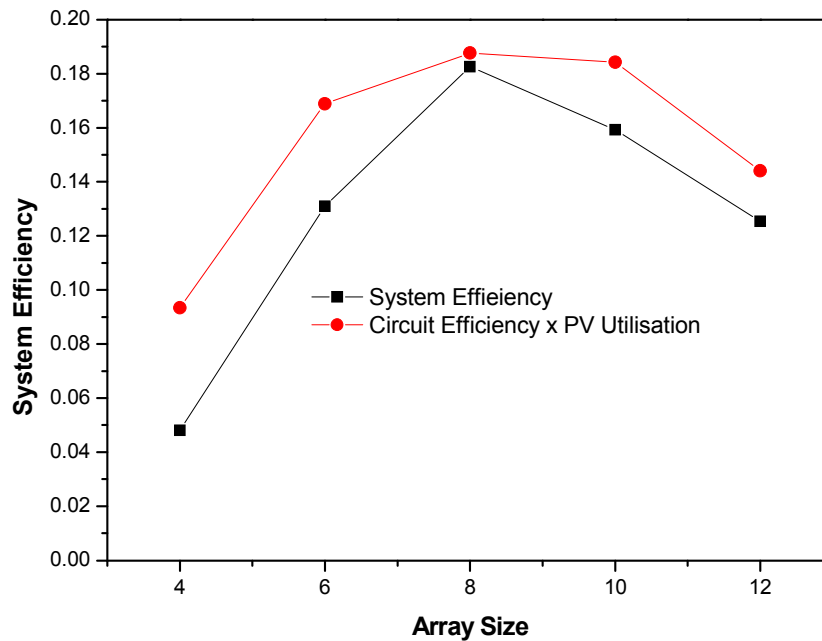
$$\eta_{\text{System}} = \frac{Power_{out}}{Power_{PV \text{ Max}}} = \frac{I_{out} \times V_{out}}{Power_{PV \text{ Max}}} \quad (6.4)$$

where  $Power_{PV \text{ Max}}$  is the maximum power output of the PV array. The light intensity resulted in a short circuit current of  $I_{sc} = 1.5\mu\text{A}$  in PV devices of  $100\mu\text{m} \times 100\mu\text{m}$ , corresponding to a short circuit current density of  $15\text{mA}/\text{cm}^2$ . This light intensity was selected as it corresponds to a typical short circuit current density of a solar cell.

It can be seen from Figure 6-17, that the system efficiency reaches a peak value of 18%. In section 5.2.3 system efficiency was defined as the product of the circuit efficiency ( $P_{out}/P_{PV}$ ) and the PV array utilisation ( $P_{PV}/P_{pvm\text{ax}}$ ) as shown in the equation below:

$$\eta_{\text{System}}(t) = \eta_{PV}(t) \times \eta_{\text{Circuit}}(t) \quad (6.5)$$

Both circuit efficiency and PV array utilisation are time dependent and the peak system efficiency is maximised when both of their peak values coincide in the time domain. Figure 6-17 compares the product of the peak circuit efficiency and the peak PV array utilisation with the system efficiency. For an 8 cell array the product is closest (ratio of 0.973). This suggests that the peak circuit efficiency and the PV array utilisation coincide.



**Figure 6-17 Effect of PV array size on peak system efficiency**

The effect of the PV array size on the circuit efficiency and the PV array utilisation is shown in Figure 6-18 and Figure 6-19 respectively. From Figure 6-18 it can be seen that the circuit efficiency drops as the array size is increased. An increasing array size results in a higher circuit input voltage, enhancing the conduction of the shunt TFT, leading to an increase in power loss.

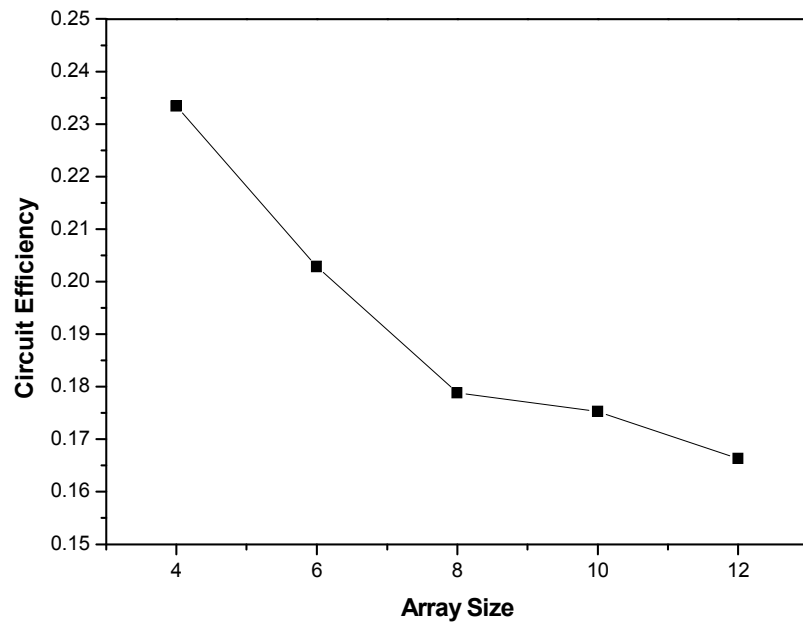


Figure 6-18 Effect of PV array size on peak circuit efficiency

Figure 6-19 shows an initial increase in the PV utilisation with an increase in the array size followed by a small reduction for array size 12.

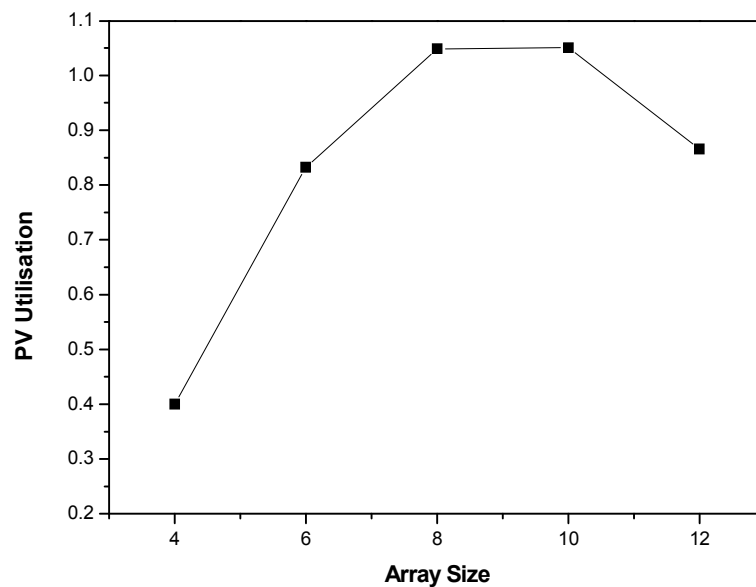


Figure 6-19 Effect of PV array size on peak PV utilisation

The PV utilisation changes depending on the operating point of the PV array, which is related to the input impedance of the circuit. Figure 6-20 shows the ratio of the PV array output voltage ( $V_{in}$ ) to the maximum power operating point voltage ( $V_{op}$ ). It can be seen that for a smaller array size (4 cell array),  $V_{in}$  is larger than  $V_{op}$ , suggesting that the cell is operating close to the  $V_{oc}$  with a small output current ( $I_{in}$ ). As the array size increases,  $V_{in}/V_{op}$  becomes smaller, approaching 1 for an 8 cell array and dropping to a value below 1 for a 12 cell array.

A smaller cell array results in a low output voltage, which in turn leads to a high resistance at the dynamic load TFT ( $T_4$  in Figure 6-15). This leads to a high input impedance of the circuit and forces the PV array to operate in the low current, high voltage range. As the PV array size and thus voltage is increased, the  $T_4$ 's resistance drops, shifting the operating point of the array closer to the  $V_{op}$  (for an 8 cell array), and to values smaller than  $V_{op}$  (for a 12 cell array).

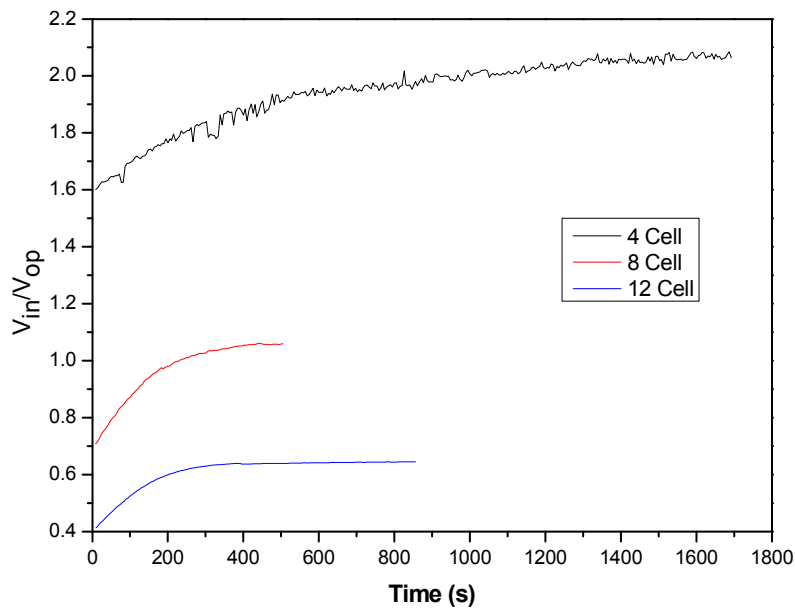
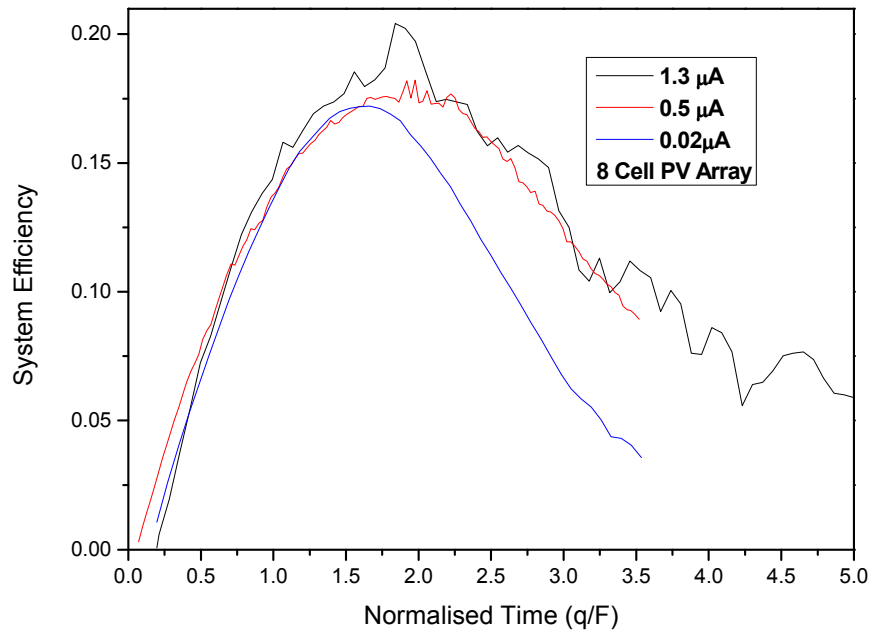


Figure 6-20 Effect of PV cell size on  $V_{in}/V_{op}$

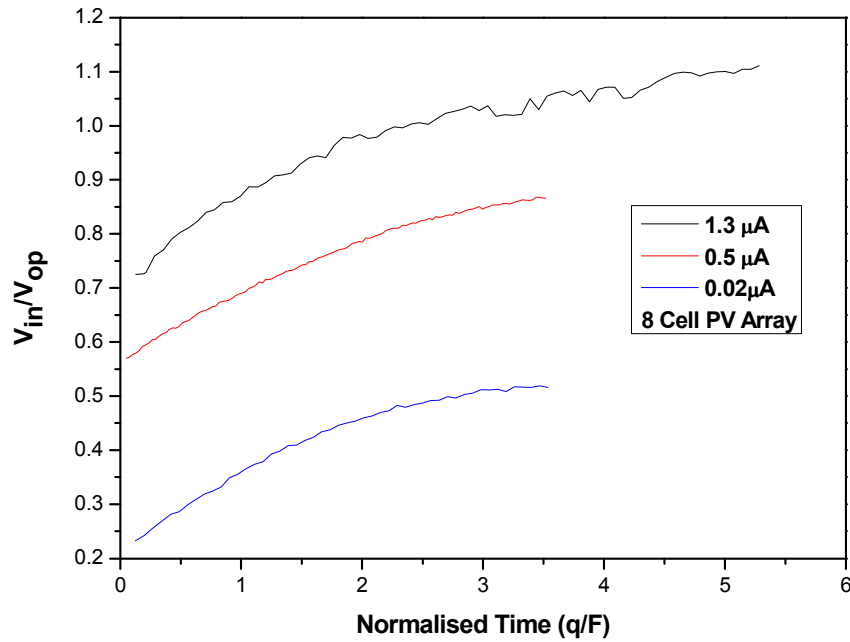
As well as array size, light intensity affects the system efficiency. Figure 6-21 shows the effect of 3 different light intensities on the peak system efficiency. The values of short circuit current are recorded for comparison. It appears that the peak system efficiency is constant regardless of the light intensity.



**Figure 6-21 Effect of light intensity on system efficiency for an 8 cell array**

The ratio of the PV array's output voltage ( $V_{in}$ ) to voltage at the maximum power point at different light intensities is plotted in Figure 6-22. The graph shows that a reduction in light intensity results in the PV array moving away from its optimum operating point and towards smaller ratios of  $V_{in}/V_{op}$ . This is due to the lower circuit input impedance, resulting in the PV array operating at values close to the  $I_{sc}$  point.





**Figure 6-22 Effect of light intensity on  $V_{in}/V_{op}$  for an 8 cell PV array**

Figure 6-23 shows the effect of light intensity on the peak circuit efficiency. It can be seen that a reduction in the light intensity, and thus in the charging current, results in an increase in the circuit efficiency. At the lower light intensities the voltage drop across the dynamic load TFT ( $T_4$ ) is smaller, leading to higher circuit efficiency. This is shown in Figure 6-24. The combined effect of reduction in PV utilisation, and an increase in the circuit efficiency with reduction in light intensity, leads to constant system efficiency as seen in Figure 6-21.

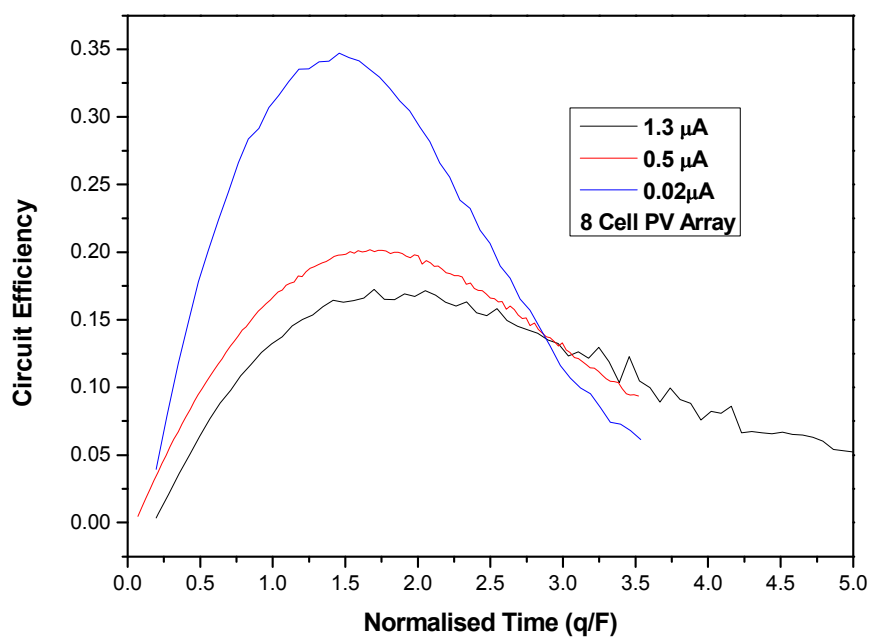


Figure 6-23 Effect of light intensity on circuit efficiency for an 8 cell array

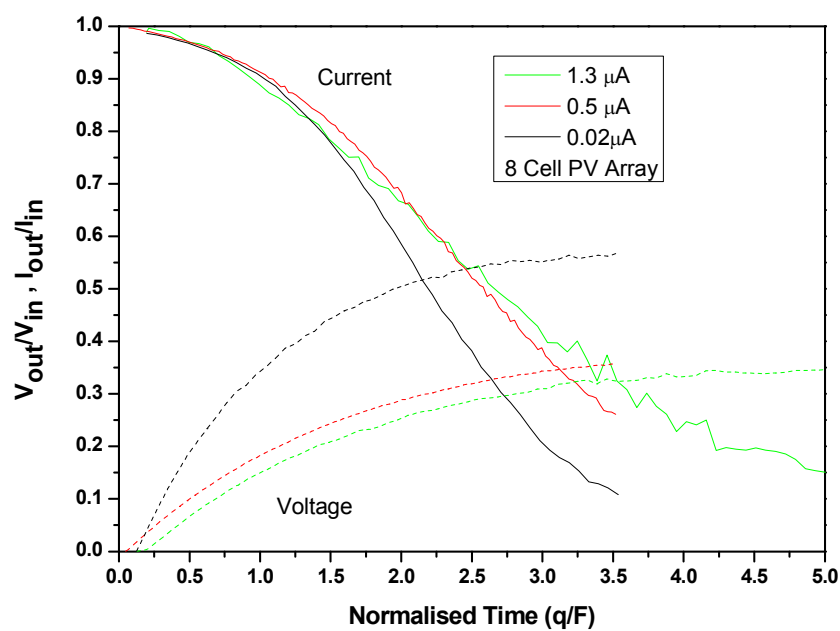


Figure 6-24 Effect of light intensity on  $V_{out}/V_{in}$  and  $I_{out}/I_{in}$  for an 8 cell array

### 6.2.3 Output Stability

In this section the stability of the circuit's output voltage with variation in the light intensity and the electrical stress is investigated. In order to decouple the effect of the PV array instability from the circuit instability, the PV array was emulated using a series of diodes (16) connected in parallel with a current source (Keithley 2400, set to  $1\mu\text{A}$ ). The stressing was performed with the capacitor removed (i.e. under fully charged load conditions) for approximately 5.6h (20,000s).

Figure 6-25 shows the variation in the input voltage with the current source's value (approximately equivalent to short circuit current and proportional to the light intensity). It shows that 2 orders of magnitude change in the current results in approximately 1V variation in the output voltage, for both pre-stress and post-stressed conditions. In Figure 6-26, the x-axis is replaced with the circuit's input voltage. The ratios of  $V_{\text{out}}/V_{\text{in}}$  are  $0.375\pm0.007$  and  $0.366\pm0.003$  for pre and post- stress respectively. The intercept points are  $0.394\pm0.02$  and  $0.560\pm0.008$  for pre and post-stress respectively.

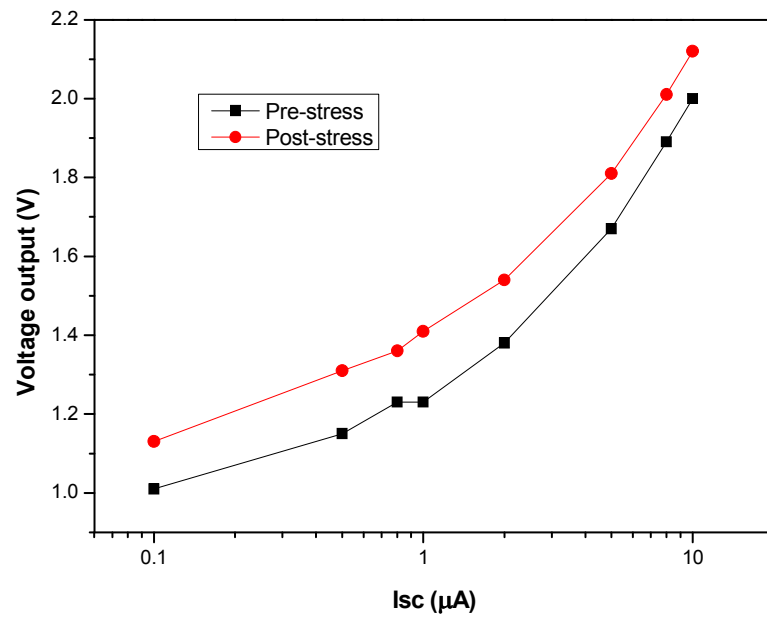


Figure 6-25 Effect of “short circuit current” on circuit’s output voltage

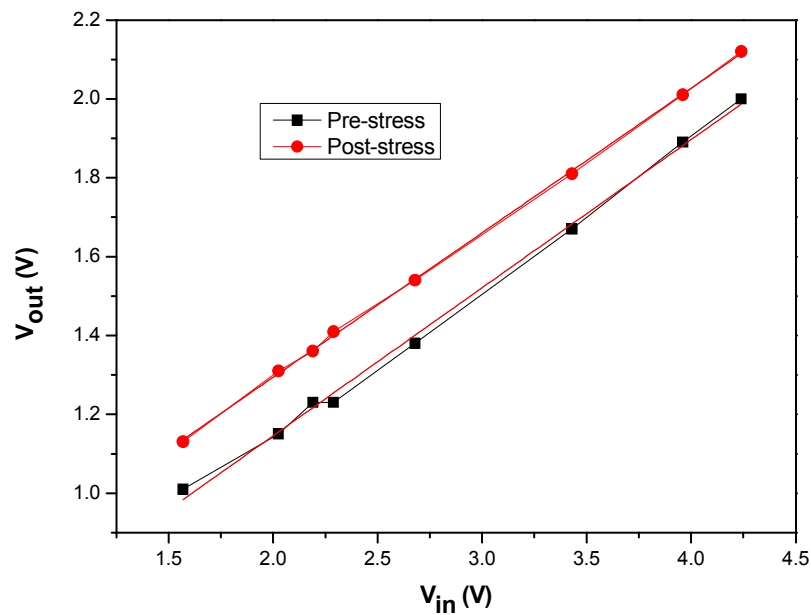


Figure 6-26 Effect of circuit input voltage on output voltage (due to variation  $I_{sc}$ )

Using the relation derived in section 5.2.2 the following can be written:

$$V_{out} = \left[1 - \frac{1}{\alpha}\right] V_{in} - \left[1 - \frac{2}{\alpha}\right] V_T \quad (6.6)$$

$$\frac{V_{out}}{V_{in}} = 0.375 \pm 0.007 = \left[1 - \frac{1}{\alpha}\right] \quad (6.7)$$

$$\xrightarrow{\text{prestress}} \alpha = 1.60 \pm 0.018$$

$$\frac{V_{out}}{V_{in}} = 0.366 \pm 0.003 = \left[1 - \frac{1}{\alpha}\right] \quad (6.8)$$

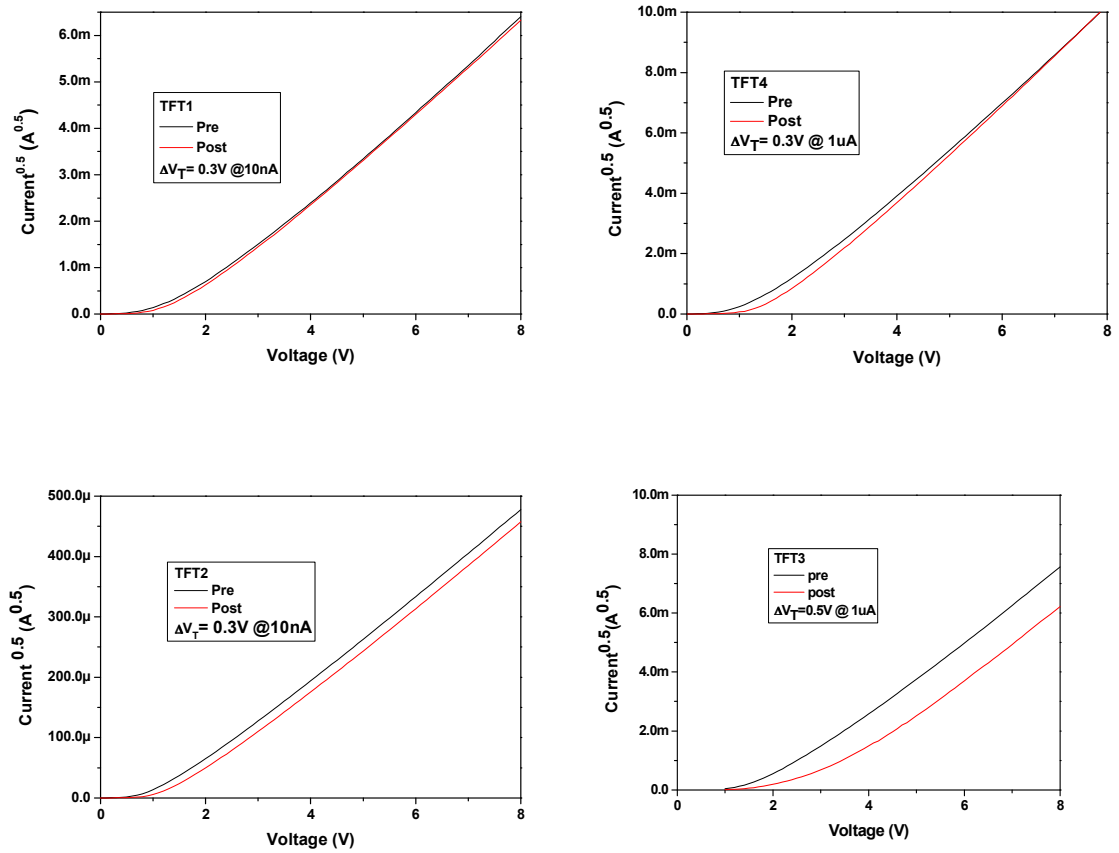
$$\xrightarrow{\text{stressed}} \alpha = 1.57 \pm 0.007$$

As expected the value of  $\alpha$  does not appear to change significantly with stressing. Figure 6-27 shows the pre and post-stressed current voltage characteristics of the TFTs. It can be seen that not all the TFTs shift by the same amount. The strongest shift comes from TFT3 (shunt TFT) with a value of 0.5V. The remainder of the TFTs shift by approximately 0.3V during the stressing cycle. Using these and  $\alpha = 1.59$  the following can be written:

$$\begin{aligned} \Delta V_{out} &= - \left[ 1 - \frac{1 + \frac{V_{T3}}{V_T}}{\alpha} \right] \Delta V_T \\ &= - \left[ 1 - \frac{1 + \frac{0.5}{0.3}}{1.59} \right] \times 0.3 = -0.2 \end{aligned} \quad (6.9)$$

Figure 6-26 shows a  $V_{out}$  shift of  $0.17 \pm 0.03V$  which is consistent with the above.

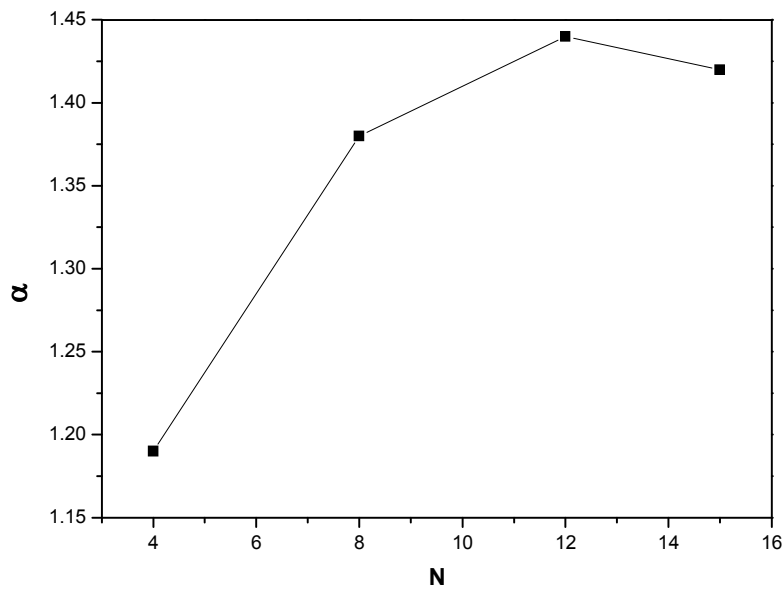
The  $\alpha$  value extracted in this section corresponds to  $K_4/K_3$  of  $1.6^2=2.56$ . However, this value does not match with the design value of  $K_4/K_3 = 7500/6000=1.25$  and thus  $\alpha = 1.12$ . The value of  $K_4/K_3$  as measured from Figure 6-27 for the pre-stressed condition is 1.26, which matches with the circuit design. This suggests that the mismatch in the theoretical and experimental results is not due to an error in the circuit's layout.



**Figure 6-27 Pre-stressed and stressed current-voltage characteristics of drain-gate connected TFTs used in the circuit**

An important assumption made in the 5.2.2 is that TFT3 operates in saturation regime. However this is only correct for a limited range of operating voltages. It is possible that the operating range used to measure input-output characteristics results in a shift of TFT3 away from saturation into linear range.

In order to check this assumption a pre-stress circuit was connected to a solar cell emulator with a different number of diodes (and therefore different  $V_{oc}$  values). The result of the measurement is shown in Figure 6-28. It can be seen that for a lower number of diodes, the value of  $\alpha$  approaches its design value ( $\alpha=1.19$  for  $N=4$ ).



**Figure 6-28 Dependence of  $\alpha$  on the number of diodes connected in series for PV emulator**

Figure 6-29 shows the variation in the output voltage with the stressing time, obtained in this experiment.

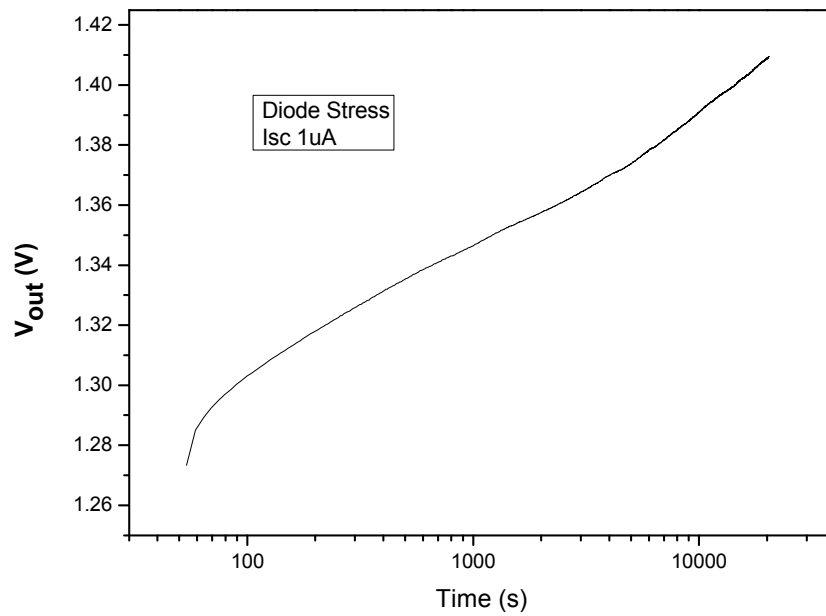


Figure 6-29 Circuit output voltage as a function of stress time

#### 6.2.4 Day-Night Cycle

The operation of the circuit with the PV array under illumination and in the dark is shown in Figure 6-30. The ratio of charging to dark durations is 0.19. In a 24h cycle this corresponds to 4.6 hours of intense sun followed by 19.4 hours of dark. A gradual drop in the output voltage can be observed during the dark cycle. This is due to the discharge of the load capacitor through the circuit and PV array. The output voltage dropped from 0.99V to 0.94 V corresponding to approximately 5%.



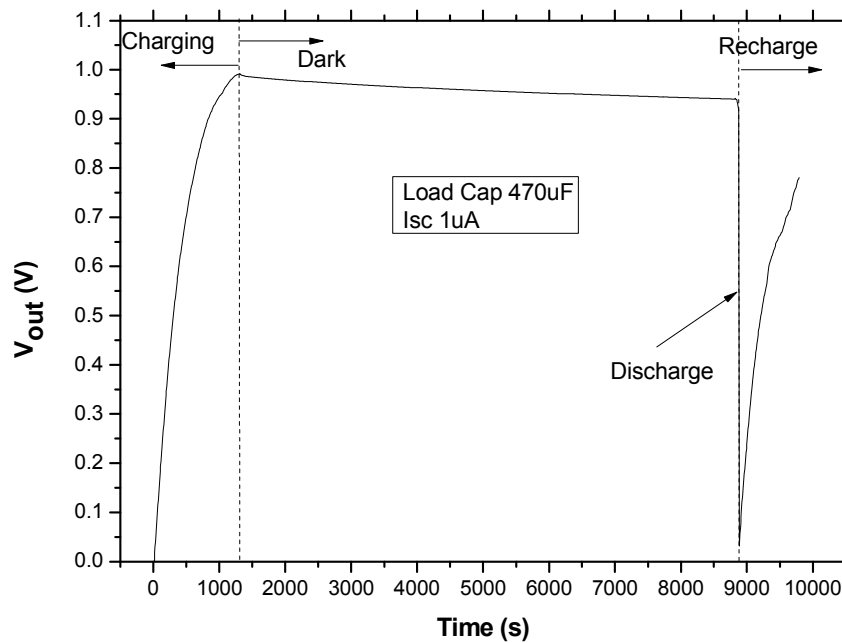


Figure 6-30 Capacitor voltage with PV array illuminated and in dark

### 6.3 Summary and Conclusions

In this chapter the result of the measurements on the PV array and circuit were presented. Photolithographically processed PV devices have a poor performance. They had a low fill factor and thus efficiency. The performance of the discrete PL processed solar cell was compared to a conventional one and possible reasons for degradation in FF were discussed. The PV array exhibited additional non-idealities. Possible reasons for their origin were proposed.

In the second part of this chapter, circuit performance was investigated. The effect of the PV array size and light intensity on the system, circuit and PV utilisation was investigated and a suitable array size identified. The effect of circuit stressing and light intensity variation on the output voltage was investigated. The results were compared with the predictions made in the previous chapter and were shown to be generally

consistent. However, some divisions existed due to the approximations made in the circuit design stage. A peak system efficiency of 18% and an average system efficiency of 11% were demonstrated in this chapter.

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## 7 Final Conclusions

In this dissertation a silicon thin film based solar energy harvesting system was presented. Thin-film deposition, fabrication of discrete devices, and the properties of a charger circuit and solar cell array were discussed.

The deposition processes for silicon based thin films have been optimised for use in TFT and Solar Cell devices. Low deposition temperature (150°C), growth of a-Si:H and nc-Si:H using SiH<sub>4</sub> diluted with H<sub>2</sub> and He has been explored. It was shown that He minimises “clustering” of the hydrogen in the silicon thin film leading to higher quality films. However the presence of excessive He led to defective, high stress films. Additional films required for the fabrication of the devices were qualified.

Two low deposition temperature effects which may influence TFT device properties were investigated:

- Contact resistance has a significant effect on the performance of the TFT. Limited fabrication temperature increases its dominance on the device and may limit the apparent device mobility. In this work an extended method of extracting contact resistance was developed and compared to the conventional method. It was shown that without accounting for the nonlinearity of contact resistance, the extracted value is an underestimate of the true device contact resistance. The influence of different contact resistance mechanisms on the field effect mobility of a-Si:H TFT was investigated.

- Dynamic instability due to mobile ion drift (or dipole polarisation) in the dielectric is explored as a possible method of improving the TFT transconductance. However, due to the difficulties with switching off the device, this approach was not used.

TFTs with a-Si:H channel material showed significantly better performance compared with nc-Si:H and therefore were used in this work. Damage to the SiN/nc-Si:H interface is one possible reason for nc-Si:H TFTs' poor performance. This can be optimised by surface treatment of the SiN in line with observations from other work [189][190][191][192]. However, further investigation should be done to confirm the nc-Si:H's quality. The a-Si:H TFTs were characterised, and it was shown that the performance was comparable to the state of the art devices.

Based on the deposition tools available, p-i-n solar cells using a-SiC:H (p-layer), a-Si:H (i-layer), and nc-Si:H (n-layer) were selected for this work. The fabrication process was optimised to minimise cross contamination and improve solar cell performance. The solar cells were characterised and it was shown that their performance was comparable to the state of the art devices.

Using the solar cell and TFT processes developed, a PV array and circuit were designed and fabricated. The PV array exhibited poor FF performance leading to low efficiency. The reason for the poor quality solar cells was attributed to the process/design related defects which can be solved by process optimisation and modification in cell layout.

The system efficiency was investigated by connecting the PV array to the circuit. Maximum system efficiency of around 18% was achieved. The system achieved in this

work has low conversion efficiency compared with the conventional designs but it has an added benefit of being a thin film with low process temperature.

Assuming PV array efficiency of 5%, average system efficiency of 11% (achieved when charging 90% of the load), and light intensity of  $500\text{W/m}^2$  over 5hours, energy of close to  $14\text{ Wh/m}^2$  can be generated. For the cell area used in this work ( $8\times 100\mu\text{m}\times 100\mu\text{m}$ ), this corresponds to  $1.12\text{ }\mu\text{Wh}$  ( $\sim 4\text{ KJoules}$ ) over a one-day period. In this work the total areas occupied by an 8 cell array and circuits were  $4.55\text{mm}^2$  and  $9\text{mm}^2$  respectively. Therefore the power density of the system was  $273\mu\text{Wh/cm}^2$ .<sup>11</sup> Comparing this value with the values estimated in section 1.2, suggests that the supercapacitor would be able to store the generated energy.

Table 7-1 shows an example of some mobile systems which could benefit from this work. It shows the average energy consumption of the device and the area of the energy harvesting required to continually run the system (based on the assumptions in the previous paragraph). The size requirement for the energy harvesting system appears to be acceptable for portable devices.

<i>Device</i>	<i>Energy consumption</i>	<i>Energy harvesting system size</i>
<i>Microfluidic flow sensor</i> [193]	$24\text{ }\mu\text{Wh}$	$0.14\text{ cm}^2$

<sup>11</sup> It should be noted that there is further scope for increasing the power density. The circuit had a large number of redundancies which are not required in a final product. Furthermore, the PV array and circuit can be vertically integrated, leading to a further reduction in product footprint.

<i>WiseMAC Sensor Node</i> [194]	168 $\mu$ Wh (7 $\mu$ W over 1000s)	0.6 cm <sup>2</sup>
<i>Portable FM radio</i> [195]	720mWh	0.43 m <sup>2</sup>
<i>Cell Phone (stand by)</i> [195]	84mW	0.5 m <sup>2</sup>

**Table 7-1 Power consumption of portable devices**

The following is a list of additional tasks which should be done to further investigate the system:

- Optimisation of PV array design and fabrication; As discussed in section 6.1.1, photolithographically (PL) processed PV cells exhibited lower efficiency compared with conventionally processed PV cells. This was attributed to the non-optimised layout design or PL process, both of which can be further optimised by investigation of the PL process and use of alternative test structure designs.
- Circuit optimisation to enhance efficiency; As discussed in section 5.2.3 higher transconductance leads to an improved circuit efficiency. This can be achieved by reducing the gate dielectric layer thickness (hence increasing the gate capacitance), using higher mobility channel material (e.g. metal-oxide semiconductors), and increasing the W/L ratio.
- Effect of temperature variation and PV instabilities on  $V_{OUT}$ ; In section 6.2.3 the effect of circuit bias stressing on  $V_{OUT}$  instability was considered. Additional sources of  $V_{OUT}$  instability are operating temperature variations and the long-term degradation of the PV array both of which should be further investigated.
- TFT circuit light shielding; Thin film silicon TFTs exhibit different characteristics under illumination compared with their standard characteristics under dark. Given that the circuit developed in this work is expected to operate under illumination, it is important block exposure of the channel to light. This

can be achieved by covering the channel area with a thick layer of non-transparent metal (the light shield). This approach is widely used for TFT circuits used in displays and would require one additional photolithography mask.

- PV array-TFT circuit integration; The ultimate aim of this project is the fabrication of an integrated thin film energy harvesting system. This would require integration of the PV array with the TFT circuit on a single substrate. This can be achieved by adopting existing fabrication processes for TFT-photodiode circuits.



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## A. AMPS 1-D

Analysis of Microelectronic and Photonic Structures (AMPS-1D) is an one dimensional device simulator. It numerically solves poisson's and continuity equations (for both holes and electrons) for given boundary conditions in one dimension. This allows the study of carrier transport in devices, including metal, semiconductors and dielectrics. AMPS-1D was used for the contact resistance analysis presented in section 3.2.

AMPS-1D allows the definition of electronic properties of the material using the density of state approach. Fig A-1 shows the density of state model selected for a-Si:H in this work.  $E_V$  and  $E_C$  are the valance and conduction bands respectively. The band-tail states are defined by the following equations:

$$G_A(E) = G_{A0} e^{\left[\frac{E-E_C}{E_A}\right]} \quad (\text{A.1})$$

$$G_D(E) = G_{D0} e^{\left[\frac{E-E_V}{E_D}\right]} \quad (\text{A.2})$$

The deep gap states are defined by two Gaussian distribution for the acceptor like states and donor like stats. Table A-1 shows the parameters selected for the intrinsic a-Si:H. The parameters are selected based on an a-Si:H model in the AMPS-1D. Table A-

2 shows the material parameters for SiN:H. In here the deep gap states are removed and the bandgap is increase to 5.3eV. Although in a true SiN:H some deep defects exist (attributed to charge traps), they are do not influence the results of this work and are thus disregarded. Table A-3 shows the material parameters for n type a-Si:H. The parameters are selected based on a n type a-Si:H model in the AMPS-1D. In here the density of acceptor like deep defect and donor density are increased.

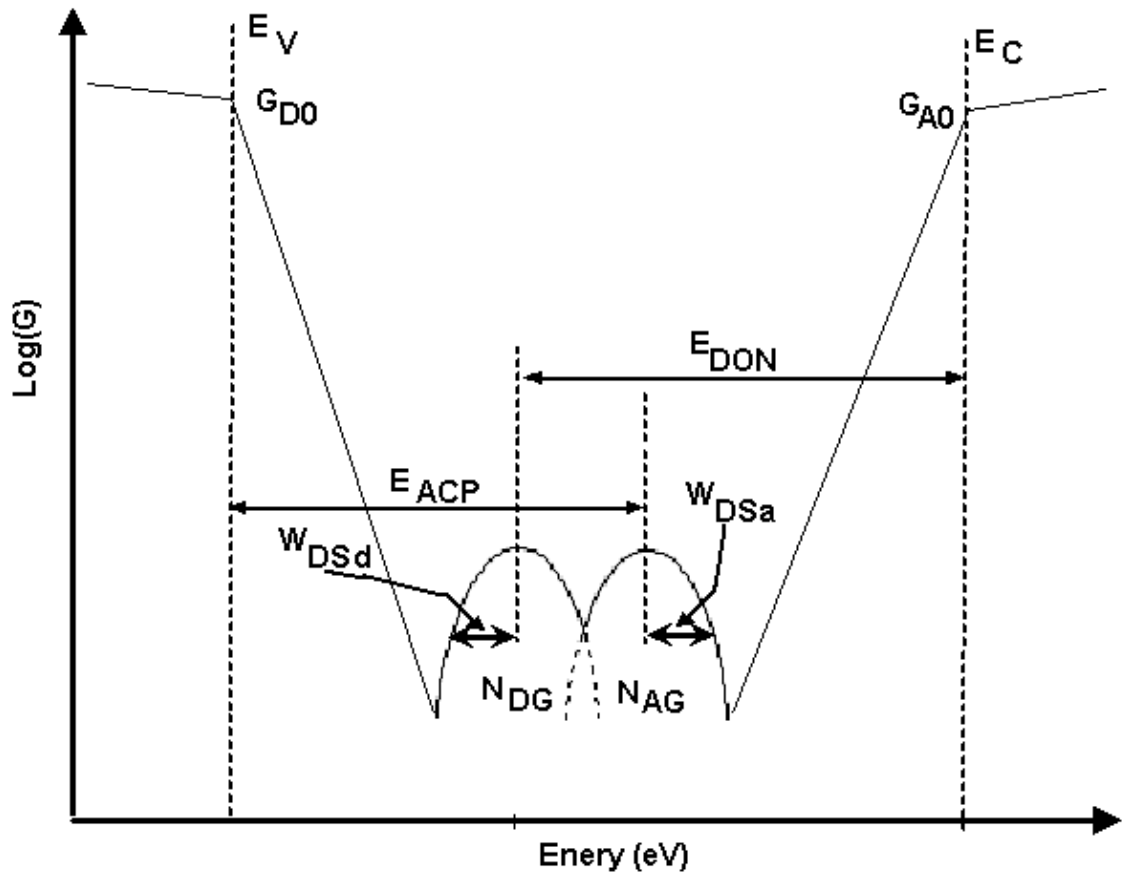


Figure A-1 Density of states diagram used for this work (adopted from AMPS-1D Manula)



Material Properties		Tail States		Deep States	
	Value	Param.	Value	Param.	Value
<i>EPS</i>	11.9	<i>ED</i>	.04 ev	<i>NDG</i>	5E+15/cm <sup>3</sup>
<i>MUN</i>	10 cm <sup>2</sup> /V/s	<i>GDO</i>	1.0E+21 /cm <sup>3</sup> .ev	<i>EDONG</i>	1.12 ev
<i>MUP</i>	1 cm <sup>2</sup> /V/s	<i>TSIG/ND</i>	1.0E-15 cm <sup>2</sup>	<i>WDSGD</i>	0.08 ev
<i>NC</i>	2.5E+20 cm <sup>3</sup>	<i>TSIG/PD</i>	1.0E-17 cm <sup>2</sup>	<i>GSIG/ND</i>	1.0 E-14 cm <sup>2</sup>
<i>NV</i>	2.5E+20 cm <sup>3</sup>	<i>EA</i>	.02 ev	<i>GSIG/PD</i>	1.0E-15 cm <sup>2</sup>
<i>NA</i>	0 /cm <sup>3</sup>	<i>GAO</i>	1.0E+21/cm <sup>3</sup> .ev	<i>NAG</i>	5.0E+15 /cm <sup>3</sup>
<i>ND</i>	<b>Variable</b> /cm <sup>3</sup>	<i>TSIG/NA</i>	1.0E-17 cm <sup>2</sup>	<i>EACPG</i>	1.02 ev
<i>EG</i>	1.82 ev	<i>TSIG/PA</i>	1.0E-15 cm <sup>2</sup>	<i>WDSAG</i>	0.08 ev
<i>CHI</i>	3.8			<i>GSIG/NA</i>	1.0E-15 cm <sup>2</sup>
				<i>GSIG/PA</i>	1.0 E-14 cm <sup>2</sup>

**Table A-1 Summary of simulation parameters used for the a-Si:H (taken from AMPS-1D 2 Gaussian model)**

Material Properties		Tail States		Deep States
	Value	Param.	Value	None
<i>EPS</i>	7.5	<i>ED</i>	0.05 ev	
<i>MUN</i>	1 cm <sup>2</sup> /V/s	<i>GDO</i>	1.0E+10 /cm <sup>3</sup> .ev	
<i>MUP</i>	1 cm <sup>2</sup> /V/s	<i>TSIG/ND</i>	1.0E-15 cm <sup>2</sup>	
<i>NC</i>	2.5E+20 cm <sup>3</sup>	<i>TSIG/PD</i>	1.0E-17 cm <sup>2</sup>	
<i>NV</i>	2.5E+20 cm <sup>3</sup>	<i>EA</i>	0.03 ev	
<i>NA</i>	0 /cm <sup>3</sup>	<i>GAO</i>	1.0E+10/cm <sup>3</sup> .ev	
<i>ND</i>	<b>0</b> /cm <sup>3</sup>	<i>TSIG/NA</i>	1.0E-17 cm <sup>2</sup>	
<i>EG</i>	5.3 ev	<i>TSIG/PA</i>	1.0E-15 cm <sup>2</sup>	
<i>CHI</i>	2 eV			

**Table A-2 Summary of simulation parameters used for the SiN**

Material Properties		Tail States		Deep States	
	Value	Param.	Value	Param.	Value
<i>EPS</i>	11.9	<i>ED</i>	.04 ev	<i>NDG</i>	1E+18/cm <sup>3</sup>
<i>MUN</i>	10 cm <sup>2</sup> /V/s	<i>GDO</i>	1.0E+21	<i>EDONG</i>	1.12 ev
<i>MUP</i>	1 cm <sup>2</sup> /V/s	<i>TSIG/ND</i>	1.0E-15 cm <sup>2</sup>	<i>WDS DG</i>	0.15 ev
<i>NC</i>	2.5E+20 cm <sup>3</sup>	<i>TSIG/PD</i>	1.0E-17 cm <sup>2</sup>	<i>GSIG/ND</i>	1.0E-14 cm <sup>2</sup>
<i>NV</i>	2.5E+20 cm <sup>3</sup>	<i>EA</i>	.02 ev	<i>GSIG/PD</i>	1.0E-15 cm <sup>2</sup>
<i>NA</i>	0 /cm <sup>3</sup>	<i>GAO</i>	1.0E+21/cm <sup>3</sup> .ev	<i>NAG</i>	1E+18 /cm <sup>3</sup>
<i>ND</i>	1E+18 /cm <sup>3</sup>	<i>TSIG/NA</i>	1.0E-17 cm <sup>2</sup>	<i>EACPG</i>	1.02 ev
<i>EG</i>	1.8 ev	<i>TSIG/PA</i>	1.0E-15 cm <sup>2</sup>	<i>WDSAG</i>	0.15 ev
<i>CHI</i>	3.8			<i>GSIG/NA</i>	1.0E-15 cm <sup>2</sup>
				<i>GSIG/PA</i>	1.0E-14 cm <sup>2</sup>

**Table A-3 Summary of simulation parameters used for the n type a-Si:H (taken from AMPS-1D  
2 Gaussian model)**